ELEC446
Advanced Computer Engineering
S1 Day 2016
Dept of Engineering

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General Information

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Credit points
3

Prerequisites
60cp including (ELEC342(P) and ELEC343(P))

Corequisites

Co-badged status
ELEC646

Unit description
This unit integrates prior learning in a specialist area of engineering with problem solving, emerging technology and aspects of engineering application, technical reporting and self-management to prepare students to work at a professional capacity. The unit aims to address the application of fundamental principles and methods at an advanced level in the context of standards and practices, modelling, analysis, design and practical implementation. The unit also develops skills in the critical evaluation of information, software and sources of error, and experimental methods. Learning will be achieved using case studies, laboratories, presentations, group work and traditional lecture format. The specific topics will focus on current advances in the area such as FPGA design, digital microelectronics, digital arithmetics, and software CAD tools.

Important Academic Dates
Information about important academic dates including deadlines for withdrawing from units are available at http://students.mq.edu.au/student_admin/enrolmentguide/academicdates/
Learning Outcomes

1. Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
2. Understand the effect of parasitics and loading on CMOS circuit performance.
3. Be able to design leaf cells for standard-cell and full-custom projects.
4. Be able to estimate complementary CMOS circuit performance, size and noise margin.
5. Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
6. Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment Tasks

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<td>Schematics in ASIC Design</td>
<td>8%</td>
<td>Week 2 and 3</td>
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<td>Layouts in ASIC Design</td>
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<td>Full Adder</td>
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<td>ASIC Design Report</td>
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Schematics in ASIC Design

Due: Week 2 and 3
Weighting: 8%

Design and test a schematic circuit for a logic gate. Complete and test a schematic circuit for a module in a larger system.

This Assessment Task relates to the following Learning Outcomes:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
Layouts in ASIC Design
Due: Week 4 and 5
Weighting: 8%

Design and test the layout for the logic gate that was assigned to you in Practical 1. Complete and test the layout for a module in a larger system.

This Assessment Task relates to the following Learning Outcomes:
• Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
• Understand the effect of parasitics and loading on CMOS circuit performance.
• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.

HSPICE
Due: Week 6 and 7
Weighting: 8%

Perform HSPICE simulations of logic circuits.

This Assessment Task relates to the following Learning Outcomes:
• Understand the effect of parasitics and loading on CMOS circuit performance.
• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.

Full Adder
Due: Week 9 and 10
Weighting: 8%

Design and test the schematic and layout circuit for a Full Adder (FA). We will use Electric for the design and HSPICE to measure the different characteristics of the circuit.

This Assessment Task relates to the following Learning Outcomes:
• Understand the effect of parasitics and loading on CMOS circuit performance.
• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.
• Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
• Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Ripple Carry Adder

Due: Week 11 and 12
Weighting: 8%

Design and test the schematic and layout circuit for a 4-bit Ripple Carry Adder (RCA). The FA cell designed in Practical 4 will be used to construct the RCA. We will use Electric for the design of the circuit and HSPICE to measure the different characteristics of the circuit.

This Assessment Task relates to the following Learning Outcomes:
• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.
• Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
• Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

ASIC Design Report

Due: Week 13
Weighting: 10%

Report on each student's customized adder design.

This Assessment Task relates to the following Learning Outcomes:
• Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
• Understand the effect of parasitics and loading on CMOS circuit performance.
• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.
• Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
• Understand fundamental microelectronic datapath design, including variations of adders and multipliers.
Exam

Due: exam date
Weighting: 50%

2 hour closed book exam.

This Assessment Task relates to the following Learning Outcomes:

• Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
• Understand the effect of parasitics and loading on CMOS circuit performance.
• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.
• Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
• Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Delivery and Resources


Notes for the “practical” sessions will be handed out in each session.

Link to the University’s honesty policy: www.student.mq.edu.au/plagiarism

Link to the University’s special consideration policy: www.reg.mq.edu.au/Forms/APScons.pdf

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central. Students should be aware of the following policies in particular with regard to Learning and Teaching:

Academic Honesty Policy http://mq.edu.au/policy/docs/academic_honesty/policy.html


In addition, a number of other policies can be found in the Learning and Teaching Category of Policy Central.

**Student Code of Conduct**

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: [https://students.mq.edu.au/support/student_conduct/](https://students.mq.edu.au/support/student_conduct/)

**Results**

Results shown in *iLearn*, or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit [ask.mq.edu.au](http://ask.mq.edu.au).

No extensions will be granted. Late tasks will be accepted up to 72* hours after the submission deadline. There will be a deduction of 20%* of the total available marks made from the total awarded mark for each 24 hour period or part thereof that the submission is late (for example, 25 hours late in submission – 40% penalty). This penalty does not apply for cases in which an application for special consideration is made and approved.

**Student Support**

Macquarie University provides a range of support services for students. For details, visit [http://students.mq.edu.au/support/](http://students.mq.edu.au/support/)

**Learning Skills**

Learning Skills ([mq.edu.au/learningskills](http://mq.edu.au/learningskills)) provides academic writing resources and study strategies to improve your marks and take control of your study.

- **Workshops**
- **StudyWise**
- **Academic Integrity Module for Students**
- **Ask a Learning Adviser**

**Student Enquiry Service**

For all student enquiries, visit Student Connect at [ask.mq.edu.au](http://ask.mq.edu.au)
Equity Support
Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

IT Help
For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

Discipline Specific Knowledge and Skills
Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- Schematics in ASIC Design
- Layouts in ASIC Design
- HSPICE
- ASIC Design Report
- Exam
Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- HSPICE
- Full Adder
- Ripple Carry Adder
- Exam

Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.

Assessment tasks

- Full Adder
- Ripple Carry Adder
We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

**Learning outcomes**

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.

**Assessment tasks**

- HSPICE
- Ripple Carry Adder
- ASIC Design Report
- Exam

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

**Learning outcomes**

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.
Assessment tasks

- Schematics in ASIC Design
- Layouts in ASIC Design
- HSPICE
- ASIC Design Report
- Exam

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- Full Adder
- Ripple Carry Adder
- Exam

Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

Learning outcome

- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
Assessment task

• ASIC Design Report

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Learning outcome

• Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.

Assessment task

• ASIC Design Report

Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcomes

• Be able to design leaf cells for standard-cell and full-custom projects.
• Be able to estimate complementary CMOS circuit performance, size and noise margin.
• Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

• HSPICE
• Ripple Carry Adder
• ASIC Design Report