ENGG141

Digital Fundamentals and Numerical Techniques

S2 Day 2016

Dept of Engineering

Contents

General Information

Unit convenor and teaching staff
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Credit points
3

Prerequisites

Corequisites

Co-badged status

Unit description
This unit aims to provide an understanding of digital fundamentals to form a foundation for study programs in science, technology, computing and engineering. The unit is also suitable for programs in commerce, finance, economics, law, and arts as an introduction to the technology of computer systems. Topics in this unit, including associated laboratory work, cover: basic theory; digital devices; and procedures for the analysis and synthesis of digital circuits and systems. The unit aims to give an appreciation of hardware aspects of design, and provides the foundations for more advanced units on Programmable Logic Design, Computer Hardware and Digital Systems Design. The unit includes six presentations providing overviews of key areas of digital technology.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

> Ability to convert between a range of numbering systems and to understand the functionality of logic gates.

Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.
Understand Latches and Flip-Flops and be able to use them to construct a range of circuits requiring memory capability such as Counters and Registers.
Ability to synthesise "combinational circuits" given "truth tables", and synthesise "sequential circuits" given "state transition diagrams"
Able to connect digital logic circuits together in a laboratory setting, ensure that the circuits operate correctly, apply test inputs and understand and evaluate the circuits outputs and operation

General Assessment Information

Student Responsibilities

Be familiar with University policy and College procedures and act in accordance with those policy and procedures.

It is the responsibility of the student to retain a copy of any work submitted. Students must produce these documents upon request. Copies should be retained until the end of the grade appeal period each term.

Student is to perform the required due diligent for their assessment grade and rectify as soon as possible upon finding any errors.

Notifications

Formal notification of assessment tasks, grading rubrics and due dates will be posted on iLearn. Although all reasonable measures to ensure the information is accurate, The University reserves the right to make changes without notice. Each student is responsible for checking iLearn for changes and updates.

Assignment Tasks

Assignment Problems will be posted on iLearn at least two weeks before their submission date.

Assignment solutions will be posted within one week after the submission date. Submissions will not be accepted once the solution is posted.

All assignments must be submitted electronically through iLearn (in pdf format). Submissions are expected to be typed set in a logical layout and sequence. Markers WILL NOT grade poorly organized or illegible scans or drafts. The expected workload includes preparation of final copies and clear diagrams.

Resubmissions will be permitted up to due date.

Late submissions or absences laboratories will not be accepted without prior arrangement made at least one week before the submission date. Extenuating circumstances will be considered upon lodgement of a formal notice of disruption to studies.

Late assignment submissions will incur a 20% reduction in marks per day.

Hurdle Requirement

The final examination is a hurdle requirement because it is the only reliable assessment of individual performance for this unit. A passing grade of 50% or more in the final examination is a condition of passing this unit. Students who make a serious attempt but fail to meet the hurdle requirement will be given one further opportunity to pass. A serious attempt is defined as achievement of a mark of 40% or greater.

Assessment Tasks

Name	Weighting	Due
1st Assignment	5%	Week 4
2nd Assignment	5%	Week 7
3rd Assignment	5%	Week 9
4th Assignment	5%	Week 12
Practicals	25%	Continual
Final examination	55%	Examination period

1st Assignment

Due: **Week 4**
Weighting: **5%**

Solutions to assignment problems based on the learning outcome is to be submitted before the due date. The assignments problems will be set to develop learning outcomes during the lecture block associated with the laboratory. Grading will take into consideration the level of understanding demonstrated as evidenced by the approach taken to present each solution.

On successful completion you will be able to:

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.

2nd Assignment

Due: **Week 7**
Weighting: **5%**

Solutions to assignment problems.

On successful completion you will be able to:

- Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.

3rd Assignment

Due: **Week 9**
Weighting: **5%**

Solutions to assignment problems.

On successful completion you will be able to:

- Understand Latches and Flip-Flops and be able to use them to construct a range of circuits requiring memory capability such as Counters and Registers.

4th Assignment

Due: **Week 12**
Weighting: **5%**

Solutions to assignment problems.

On successful completion you will be able to:

- Ability to synthesise "combinational circuits" given "truth tables", and synthesise "sequential circuits" given "state transition diagrams"

Practicals

Due: **Continual**
Weighting: **25%**

Participation in Practicals counts toward this mark. The mark will be assessed during scheduled Practicals. Grading will take into consideration the level of participation as evidenced by attendance and demeanour in the classes. High marks will be awarded for initiative, approach to self-learning and self-management. Students are expected to participate in the learning activities with a developing level of independence as well as team work.

On successful completion you will be able to:

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.
- Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.
- Understand Latches and Flip-Flops and be able to use them to construct a range of circuits requiring memory capability such as Counters and Registers.
- Ability to synthesise "combinational circuits" given "truth tables", and synthesise

"sequential circuits" given "state transition diagrams"

- Able to connect digital logic circuits together in a laboratory setting, ensure that the circuits operate correctly, apply test inputs and understand and evaluate the circuits outputs and operation

Final examination

Due: **Examination period**
Weighting: **55%**

A final closed-book examination of three hours will be conducted during the formal examination period.

No calculators will be allowed during this examination.

This task is a hurdle requirement. A passing grade of 50% or more in the final examination is a condition of passing this unit.

On successful completion you will be able to:

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.
- Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.
- Understand Latches and Flip-Flops and be able to use them to construct a range of circuits requiring memory capability such as Counters and Registers.
- Ability to synthesise "combinational circuits" given "truth tables", and synthesise "sequential circuits" given "state transition diagrams"

Delivery and Resources

Required unit materials:

- Text book
- Tutorial and laboratory notes

Textbook

Floyd, T. L. "Digital Fundamentals", 10th ed, (Pearson Prentice-Hall, 2009)

Reference books

Another book that follows the treatment of ENGG141 closely is:

Tocci, Widmer and Moss, "Digital systems: principles and applications", 10th ed (Pearson Prentice-Hall)

Notes

Tutorial and laboratory notes for practical tutorial session are available on iLearn. Each student is required to print out the lab notes before each Practical.

Recommended readings

- Floyd, Chapters 1-9 (covered in detail)
- Floyd, Chapters 10, 11, 13 (overview lectures)

Technology used and required

Logic trainers for digital fundamentals and small/medium-scale integrated circuits. Access to a computer device to access iLearn, view video modules, and complete online quizzes.

Online lectures

Except for the first lecture in Week 1, all lecture material will be delivered as as online video modules (similar to youtube) through iLearn . Each module is approximately from 5 min to 15 min in duration with a number of modules comprising a topic. Students will be required to view the video modules that are identified for that week and then answer a short online quiz for each module. Lectures slides are also available for viewing.

Video modules (online lectures)

Watching the online lectures and completing the quizzes will be considered as pre-work for the practical session and therefore be part of the practical assessment mark.

Tutorial/practical sessions

There are ten practical sessions (each of three hours duration) starting in Week 3. Students will work in groups of two, and will attend one practical session in each week. Most practical sessions will contain both tutorial work and laboratory work. Students are advised to attempt the tutorial work before attending each practical session.

On the completion of each session, each group must complete and submit a “check-list” that itemizes each section of tutorial and laboratory work. Each item is to be initialed by the group members on completion of the work. The check-list will also have (on its reverse side) one problem for which the group must solve. Your ability to solve this problem is considered an important “outcome” of the practical. Your performance as recorded in your copies of the practical notes and summarized by your check-list will be used in the assessment of your practical work. Students with work in groups but will be marked individually.

Food and drink are not permitted in the laboratory. Students will not be permitted to enter the laboratory without appropriate footwear. Thongs and sandals are not acceptable.

Tutor consultation

Tutor consultation time will be Tuesday between 2 and 4pm or by appointment.

Unit Schedule

Week	Topics	Practicals	Lecturer
1	Introductory digital concepts Number systems	No practical	BM/Online
2	Code conversion, binary arithmetic, Logic functions and IC logic gates	No practical	Online
3	Boolean algebra and logic identities	Practical 1 Number systems & logic gates	Online
4	K-maps and logic simplification using K-maps	Practical 2 Boolean algebra & logic gates	Online
5	Combinational logic Adders, subtractors	Practical 3 K-maps, logic minimisation and circuit implementation	Online
6	Comparators Multiplexers/demultiplexers	Practical 4 Combinational circuit implementation using integrated circuits	Online
7	Latches	Practical 5 XOR gate applications	Online
8	Edge-triggered flip-flops	Practical 6 Encoder/decoder circuit	Online
9	Asynchronous counters	Practical 7 Flip-flops	Online
10	Synchronous binary counters	Practical 8 Binary counters & multiplexer/demultiplexer circuit	Online

11	Synchronous counter analysis and design	Practical 9 Synchronous counter design (1)	Online
12	Shift registers	Practical 10 Synchronous counter design (2)	Online
13	Revision	Revision	BM

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central. Students should be aware of the following policies in particular with regard to Learning and Teaching:

Academic Honesty Policy http://mq.edu.au/policy/docs/academic_honesty/policy.html

New Assessment Policy in effect from Session 2 2016 http://mq.edu.au/policy/docs/assessment/policy_2016.html. For more information visit http://students.mq.edu.au/events/2016/07/19/new_assessment_policy_in_place_from_session_2/

Assessment Policy prior to Session 2 2016 http://mq.edu.au/policy/docs/assessment/policy.html

Grading Policy prior to Session 2 2016 http://mq.edu.au/policy/docs/grading/policy.html

Grade Appeal Policy http://mq.edu.au/policy/docs/gradeappeal/policy.html

Complaint Management Procedure for Students and Members of the Public http://www.mq.edu.au/policy/docs/complaint_management/procedure.html

Disruption to Studies Policy http://www.mq.edu.au/policy/docs/disruption_studies/policy.html *The Disruption to Studies Policy is effective from March 3 2014 and replaces the Special Consideration Policy.*

In addition, a number of other policies can be found in the Learning and Teaching Category of Policy Central.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/support/student_conduct/

Results

Results shown in *iLearn*, or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au.

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.
- Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.
- Understand Latches and Flip-Flops and be able to use them to construct a range of

circuits requiring memory capability such as Counters and Registers.

- Ability to synthesise "combinational circuits" given "truth tables", and synthesise "sequential circuits" given "state transition diagrams"
- Able to connect digital logic circuits together in a laboratory setting, ensure that the circuits operate correctly, apply test inputs and understand and evaluate the circuits outputs and operation

Assessment tasks

- 1st Assignment
- 2nd Assignment
- 3rd Assignment
- 4th Assignment
- Practicals
- Final examination

Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

Learning outcome

- Able to connect digital logic circuits together in a laboratory setting, ensure that the circuits operate correctly, apply test inputs and understand and evaluate the circuits outputs and operation

Assessment task

- Practicals

Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcome

- Able to connect digital logic circuits together in a laboratory setting, ensure that the circuits operate correctly, apply test inputs and understand and evaluate the circuits outputs and operation

Assessment task

- Practicals

Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.
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Assessment tasks

- 1st Assignment
- 2nd Assignment
- 3rd Assignment
- 4th Assignment
- Practicals
- Final examination

Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

Learning outcomes

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.
- Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.
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Assessment tasks

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- 2nd Assignment
- 3rd Assignment
- 4th Assignment
- Practicals
- Final examination

Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Ability to convert between a range of numbering systems and to understand the functionality of logic gates.
- Ability to apply Boolean identities and Karnaugh maps to the minimisation of digital circuits and an understanding of Multiplexers, Comparators and Parity.
- Understand Latches and Flip-Flops and be able to use them to construct a range of circuits requiring memory capability such as Counters and Registers.
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Assessment tasks

- 1st Assignment
- 2nd Assignment
- 3rd Assignment
- 4th Assignment
- Practicals
- Final examination

Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcome

- Able to connect digital logic circuits together in a laboratory setting, ensure that the circuits operate correctly, apply test inputs and understand and evaluate the circuits outputs and operation

Assessment tasks

- Practicals
- Final examination

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Assessment task

- Practicals