ELEC241

Programmable Logic Design

S2 Day 2014

Dept of Engineering

Contents

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General Information

Unit convenor and teaching staff
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Credit points
3

Prerequisites
12cp including (ELEC141(P) or ENGG141(P) or ELEC274(P))

Corequisites

Co-badged status

Unit description
This unit introduces some of the hardware components and software tools used to design digital systems, particularly those popular Programmable Logic Devices. For systems of moderate complexity we choose to use Generic Array Logic devices (GALs) and simple software based on Boolean equations (OPALjr). Some set practical exercises are performed individually, while teams are formed to work on a larger project which spans some weeks.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

Ability to evaluate alternative designs of digital systems that have been implemented with programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability

Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection

Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system

Ability to apply logic design procedures and development software for programmable

logic devices for implementing finite state machines (including traffic light controllers)
Basic understanding of applications and performance capabilities of programmable logic devices
Knowledge of programmable logic devices (in particular GALs): families, architecture
Cooperative work within an integrated team

General Assessment Information

Group practical

Practical 1 performance 3%
Practical 2 performance 3%
Practical 3 performance 3%
Practical 4 performance 3%
Practical 5 performance 3%
Total 15%

Team project

Practical 6-10 attendance 5%
Project deliverable 6%
Final report 7%
Presentation 7%
Total 25%

Exam (one 3-hour closed-book exam) 60 %

Total 100%

Assessment Tasks

Name	Weighting	Due
Practical 1	3%	Week 2
Practical 2	3%	Week 3
Practical 3	3%	Week 4
Practical 4	3%	Week 5

Name	Weighting	Due
Practical 5	3%	Week 6
Practical 6	1%	Week 7
Practical 7	1%	Week 8
Practical 8	1%	Week 9
Practical 9	1%	Week 10
Practicel 10	1%	Week 11
Project Deliverable	6%	Week 12
Final Report	7%	Week 12
Presentation	7%	Weel 12
Exam	60%	Week 14

Practical 1

Due: **Week 2**
Weighting: **3%**

Practical 1 – PLD Implementation of Shift Register Circuits

On successful completion you will be able to:

- Ability to evaluate alternative designs of digital systems that have been implemented with programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability
- Basic understanding of applications and performance capabilities of programmable logic devices
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Practical 2

Due: **Week 3**
Weighting: **3%**

Practical 2 – PLD Implementation of Synchronous Cascadable Counters

On successful completion you will be able to:

- Ability to evaluate alternative designs of digital systems that have been implemented with

programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability
- Basic understanding of applications and performance capabilities of programmable logic devices
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Practical 3

Due: **Week 4**
Weighting: **3%**

Practical 3 – Design and Implementation of a Traffic Light Controller, and Design and Implementation of MOD-n Counters with Single-Cycle Operation

On successful completion you will be able to:
- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)

Practical 4

Due: **Week 5**
Weighting: **3%**

Practical 4 – Boundary Scan Testing with Signature Analysis

On successful completion you will be able to:
- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)

Practical 5

Due: **Week 6**
Weighting: **3%**

Practical 5 – Boundary Scan Testing with Signature Analysis

On successful completion you will be able to:

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)

Practical 6

Due: **Week 7**
Weighting: **1%**

Practical 6 – Traffic Light Controller Design and implementation

(GAL – Team Project)

On successful completion you will be able to:

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Cooperative work within an integrated team

Practical 7

Due: **Week 8**
Weighting: **1%**

Practical 7 – Traffic Light Controller Design and implementation

(GAL – Team Project)

On successful completion you will be able to:

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Cooperative work within an integrated team

Practical 8

Due: **Week 9**
Weighting: **1%**

Practical 8 – Traffic Light Controller Design and implementation

(GAL – Team Project)

On successful completion you will be able to:

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Cooperative work within an integrated team

Practical 9

Due: **Week 10**
Weighting: **1%**

Practical 9 – Traffic Light Controller Design and implementation

(GAL – Team Project)

On successful completion you will be able to:

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Cooperative work within an integrated team

Practicel 10

Due: **Week 11**
Weighting: **1%**

Practical 10 – Traffic Light Controller Design and implementation

(GAL – Team Project)

On successful completion you will be able to:

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Cooperative work within an integrated team

Project Deliverable

Due: **Week 12**

Weighting: **6%**

Project Deliverable

On successful completion you will be able to:

- Cooperative work within an integrated team

Final Report

Due: **Week 12**
Weighting: **7%**

Final Report

On successful completion you will be able to:

- Cooperative work within an integrated team

Presentation

Due: **Weel 12**
Weighting: **7%**

Presentation

On successful completion you will be able to:

- Cooperative work within an integrated team

Exam

Due: **Week 14**
Weighting: **60%**

Exam (one 3-hour closed-book exam)

On successful completion you will be able to:

- Ability to evaluate alternative designs of digital systems that have been implemented with programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability
- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Basic understanding of applications and performance capabilities of programmable logic devices

- Knowledge of programmable logic devices (in particular GALs): families, architecture

Delivery and Resources

Lectures	There are two lectures per week. Lecture topics are provided in the (attached) timetable. Lecture notes containing the figures and other information used in the presentation of most lectures are available on Blackboard. Students are advised to print a copy of these notes before each lecture so that their personal copies may be annotated during the course of the lecture. From time to time, important announcements and notices will be made in the lectures. It is the responsibility of the student to be aware of these announcements and notices.
Assignments	None
Tutorial/ practical sessions	There are ten practical sessions (each of three hours duration) starting in Week 2. Students will work in groups of two or teams of four and will attend one practical session in each week. On the completion of each session, each group/team must complete and submit a "check-list" that itemizes each section of tutorial and laboratory work. Each item is to be initialed by the group members on completion of the work. Your performance as recorded in your copies of the practical notes and summarized by your check-list will be used in the assessment of your practical work. Food and drink are not permitted in the laboratory. Students will not be permitted to enter the laboratory without appropriate footwear. Thongs and sandals are not acceptable.
Laboratory note book	Each student must have a bound exercise book to be used as a tutorial/laboratory note book. This book is to be used for any preliminary work for the laboratory sessions and for any designs or results recorded during these sessions. On the completion of each session note book entries must be signed and dated by a tutor.
Reports	A final report based on the team project is required from each team (not each team member). The report should be submitted by *24th October, 2013 (the Thursday in week 11)*.
Summary of the assessment tasks students must undertake to demonstrate their learning	Group practical Practical 1 performance 3% Practical 2 performance 3% Practical 3 performance 3% Practical 4 performance 3% Practical 5 performance 3% Total 15% Team project Practical 6-10 attendance 5% Project deliverable 6% Final report 7% Presentation 7% Total 25% Exam (one 3-hour closed-book exam) 60 % Total 100%

What is required to complete the unit satisfactorily	Pass mark in each of the assessment components (practicals, team project, report, presentation and examination)
Extension requests	Must be supported by evidence of medical conditions or misadventure.
Examination conditions	3-hour, closed book
Supplementary examination	Applications for a supplementary examination (based on medical reasons or misadventure) will only be considered if students have gained passes in the practicals, reports and presentation.
Grades and Final Mark	The grades of Credit, Distinction and High Distinction will be determined by setting “break-points” between Pass/Credit, Credit/Distinction and Distinction/High-Distinction. Linear interpolation will be used between break-points. Performance in all of the assessment components (practicals, assignments and examination) will be used to set the break-points.
Text book	None
Reference book(s)	Tocci, R. J., “Digital Systems -- Principles and Applications”, 10th ed, Prentice Hall 2010, Chpater 13. Floyd, T. L., “Digital Fundamentals”, 10th ed., Pearson Prentice-Hall 2009. Charles, R. H. and John, L. K., “Digital Systems Design Using VHDL”, Second edition, Thompson, 2008
Notes	Notes for the practical sessions are available online. Each student is required to preview the corresponding notes before each practical session.
Required unit materials and/or recommended readings	Required unit materials: Laboratory Notes (online) Recommended readings Floyd, Chapter 11, “Programmable Logic and Software” Tocci, Chapter 13, “Programmable Logic Device Architectures”
Link to the University’s honesty policy	www.student.mq.edu.au/plagiarism
Link to the University’s special consideration policy	www.reg.mq.edu.au/Forms/APScons.pdf
Short statement about any changes made to previous offerings of the unit	No major changes to previous offerings.

Unit Schedule

Timetable

Week	Lectures	Practicals
1 (FZ)	1A – Outline 1B – Programmable Logic Devices 1C – Generic Array Logics (GALs)	
2 (FZ)	2A – Shift Register Design 2B – Applications	Practical 1 – PLD Implementation of Shift Register Circuits
3 (FZ)	3A – Counter Design and Applications 3B – Synchronous Cascadable Counters	Practical 2 – PLD Implementation of Synchronous Cascadable Counters
4 (FZ)	4A – Finite State Machines (FSM) and Timing control of FSM 4B – Traffic Light Controllers	Practical 3 – Design and Implementation of a Traffic Light Controller, and Design and Implementation of MOD-n Counters with Single-Cycle Operation
5 (FZ)	5A – Boundary Scan Testing 5B – Boundary Scan Testing	Practical 4 – Boundary Scan Testing with Signature Analysis
6 (FZ)	6A – Review of Number Systems 6B – Review of Number Systems	Practical 5 – Boundary Scan Testing with Signature Analysis
7 (FZ)	7A – Introduction to Team Project 7B – Introduction to Team Project	Practical 6 – Traffic Light Controller Design and implementation (GAL – Team Project)

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central. Students should be aware of the following policies in particular with regard to Learning and Teaching:

Academic Honesty Policy http://mq.edu.au/policy/docs/academic_honesty/policy.ht

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Assessment Policy http://mq.edu.au/policy/docs/assessment/policy.html

Grading Policy http://mq.edu.au/policy/docs/grading/policy.html

Grade Appeal Policy http://mq.edu.au/policy/docs/gradeappeal/policy.html

Grievance Management Policy http://mq.edu.au/policy/docs/grievance_management/policy.html

Disruption to Studies Policy http://www.mq.edu.au/policy/docs/disruption_studies/policy.html *The Disruption to Studies Policy is effective from March 3 2014 and replaces the Special Consideration Policy.*

In addition, a number of other policies can be found in the Learning and Teaching Category of Policy Central.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/support/student_conduct/

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

IT Help

For help with University computer systems and technology, visit http://informatics.mq.edu.au/help/.

When using the University's IT, you must adhere to the Acceptable Use Policy. The policy

applies to all who connect to the MQ network including students.

Graduate Capabilities

Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

Learning outcomes

- Ability to evaluate alternative designs of digital systems that have been implemented with programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability
- Basic understanding of applications and performance capabilities of programmable logic devices
- Knowledge of programmable logic devices (in particular GALs): families, architecture
- Cooperative work within an integrated team

Assessment tasks

- Practical 1
- Practical 2
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Project Deliverable
- Final Report
- Presentation

Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcomes

- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Basic understanding of applications and performance capabilities of programmable logic devices
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10

Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Exam

Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

Learning outcomes

- Ability to evaluate alternative designs of digital systems that have been implemented with programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability
- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Assessment tasks

- Practical 1
- Practical 2
- Practical 3

- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Exam

Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Exam

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Ability to analyse sets of Boolean equations representing the implementation of boundary scan testing of a digital system
- Ability to apply logic design procedures and development software for programmable logic devices for implementing finite state machines (including traffic light controllers)
- Knowledge of programmable logic devices (in particular GALs): families, architecture

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Exam

Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcome

- Cooperative work within an integrated team

Assessment tasks

- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Project Deliverable
- Final Report
- Presentation

Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

Learning outcomes

- Ability to evaluate alternative designs of digital systems that have been implemented with programmable logic devices based on criteria such as performance capability, hardware requirements, software aids and testability
- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Cooperative work within an integrated team

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9

- Practicel 10
- Project Deliverable
- Final Report
- Presentation

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Learning outcomes

- Ability to synthesise programmable logic devices (GALs) for the control of traffic at a complex traffic intersection
- Basic understanding of applications and performance capabilities of programmable logic devices
- Cooperative work within an integrated team

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Practical 9
- Practicel 10
- Project Deliverable
- Final Report
- Presentation

Changes since First Published

Date	Description
14/01/2014	The Prerequisites was updated.