ELEC241

Programmable Logic Design

S2 Day 2017

Dept of Engineering

Contents

General Information

Unit convenor and teaching staff
Lecturer
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Tuesday 10-12

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Credit points
3

Prerequisites
(12cp at 100 level or above) including (COMP115 or ELEC141 or ENGG141)

Corequisites

Co-badged status

Unit description
This unit introduces some of the hardware components and software tools used to design digital systems, particularly those popular Programmable Logic Devices. For systems of moderate complexity we choose to use Generic Array Logic devices (GALs) and simple software based on Boolean equations (OPALjr). Some set practical exercises are performed individually, while teams are formed to work on a larger project which spans some weeks.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays

Understand applications and performance capabilities of programmable logic devices

Ability to apply logic design procedures to programmable logic devices, such as implementing finite state machines

Ability to effectively manipulate designs of digital systems that have been implemented on programmable logic devices, based on different criteria

Demonstrate engagement to active learning as well as self-learning capability in a group manner

General Assessment Information

Student Responsibilities

Be familiar with University policy and College procedures and act in accordance with those policy and procedures.

It is the responsibility of the student to retain a copy of any work submitted. Students must produce these documents upon request. Copies should be retained until the end of the grade appeal period each term.

Student is to perform the required due diligent for their assessment grade and rectify as soon as possible upon finding any errors.

Notifications

Formal notification of assessment tasks, grading rubrics and due dates will be posted on iLearn. Although all reasonable measures to ensure the information is accurate, The University reserves the right to make changes without notice. Each student is responsible for checking iLearn for changes and updates.

Report and Assignment Tasks

Assignment Problems will be posted on iLearn at least two weeks before their submission date. Assignment solutions will be posted within a week after the submission date. Submissions will not be accepted once the solution is posted.

Assignment submissions and plagiarism policies

All assignments and reports must be submitted electronically through iLearn (in pdf format). Submissions will undergo plagiarism checkers using the turnitin software and any work deemed to have 30% or higher similarity score may incur academic penalty. For more details on the policies of academic penalties relating to academic honesty, please refer to the policies and procedures section below.

Submissions are expected to be typed set in a logical layout and sequence. Markers WILL NOT grade poorly organized or illegible scans or drafts. The expected workload includes preparation of final copies and clear diagrams.

Late submissions

Late submissions or absences from tutorials and laboratories will not be accepted without prior arrangement made at least one week before the submission date. Extenuating circumstances will be considered upon lodgement of a formal notice of disruption of studies.

Hurdle Requirement

The final exam is a hurdle requirement because it is the only reliable assessment of individual performance for this unit. A passing grade of 50% or more in the final exam is a condition of passing this unit. Students who make a serious attempt but fail to meet the hurdle required will be given one further opportunity to pass. A serious attempt is defined as achievement of a mark of 40% or greater in the examination.

Grading and passing requirement for unit

For further details about grading, please refer below in the policies and procedures section.

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD).

Final Examinations

Final examinations will typically take place at the end of the semester. For further information, please refer to the Examination Timetable website on www.mq.edu.au. Students who are allocated a supplementary examination must be available during the supplementary examination period of 11th to 15th December 2017.

Assessment Tasks

Name	Weighting	Hurdle	Due
Diagnostic Quiz	3%	No	Week 3
Practical 1 to 3 Report	5%	No	Week 4
Design Assessment	10%	No	Before Week 8
Final Report	20%	No	Week 12
Engagement	12%	No	Continuous
Exam	50%	Yes	Exam Period

Diagnostic Quiz

Due: **Week 3**
Weighting: **3%**

A diagnostic quiz to show the current level of knowledge. This is graded and feedback will be provided. This quiz is designed to provide feedback to the student about their readiness for this unit.

On successful completion you will be able to:

- Demonstrate engagement to active learning as well as self-learning capability in a group manner

Practical 1 to 3 Report

Due: **Week 4**
Weighting: **5%**

An individual report that covers your experience with the first three practicals in the unit. This report will require an evaluation of your work and an explanation of key design decisions made during these practicals.

Grading will take into consideration the level of discovery as evidenced by insight presented in the report in terms of critical evaluation of the practical activity and technical justification of procedure and design.

On successful completion you will be able to:

- Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays
- Understand applications and performance capabilities of programmable logic devices

Design Assessment

Due: **Before Week 8**
Weighting: **10%**

The design assessment requires a design of a finite state machine. This assignment will require the analysis of a design task, the designing of the logic for the task, and the implementation of the logic to satisfy the task.

Grading will take into consideration the clarity of the design decisions, and the economy of the solution.

On successful completion you will be able to:

- Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays
- Understand applications and performance capabilities of programmable logic devices
- Ability to apply logic design procedures to programmable logic devices, such as implementing finite state machines

Final Report

Due: **Week 12**
Weighting: **20%**

An individual report that covers your experience with the group project in the unit. This report will require an evaluation of your work and an explanation of key design decisions made during these practicals.

Grading will take into consideration the level of discovery as evidenced by insight presented in the report in terms of critical evaluation of the practical activity and technical justification of procedure and design. There are multiple design choices available for the major work, and clear understanding of these choices, and the rational behind the solution chosen, will need to be evidenced. Grading will take into consideration the level of understanding demonstrated as evidenced by the approach taken to solve the technical hurdles present within the limited resources available to perform the required design.

On successful completion you will be able to:

- Understand applications and performance capabilities of programmable logic devices
- Ability to apply logic design procedures to programmable logic devices, such as implementing finite state machines
- Ability to effectively manipulate designs of digital systems that have been implemented on programmable logic devices, based on different criteria

Engagement

Due: **Continuous**
Weighting: **12%**

Active engagement during scheduled practicals. This unit requires significant group work, and each group member must actively participate in the group. Grading will take into consideration the level of participation as evidenced by attendance and demeanour in the classes. High marks will be awarded for initiative, approach to self-learning and self-management. Students are expected to participate in the learning activities with a developing level of independence as well as group work.

On successful completion you will be able to:

- Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays
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Exam

Due: **Exam Period**
Weighting: **50%**

This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

Exam (one 3-hour closed-book exam)

On successful completion you will be able to:

- Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays
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Delivery and Resources

Lectures	There is one lecture per week. From time to time, important announcements and notices will be made in the lectures. It is the responsibility of the student to be aware of these announcements and notices.
Assignments	There are three written assignments required for this unit. These are individual assignments and must be submitted as pdfs. The written work must detail both group work and the individual contribution by the student.
Tutorial/ practical sessions	There are eleven practical sessions (each of three hours duration) starting in Week 2. Students will work in groups of two or teams of four and will attend one practical session in each week. On the completion of each session, each group/team must complete and submit a “check-list” that itemises each section of tutorial and laboratory work. Each item is to be initialled by the group members on completion of the work. Your performance as recorded in your copies of the practical notes and summarised by your check-list will be used in the assessment of your practical work. Food and drink are not permitted in the laboratory. Students will not be permitted to enter the laboratory without appropriate footwear. Thongs and sandals are not acceptable.
Laboratory note book	Each student must have a bound exercise book to be used as a tutorial/laboratory note book. This book is to be used for any preliminary work for the laboratory sessions and for any designs or results recorded during these sessions. On the completion of each session note book entries must be signed and dated by a tutor.
Reports	A final report based on the team project is required from each team member).
Text book	None
Reference book(s)	Floyd, T. L., “Digital Fundamentals”, 10th ed., (or later) Pearson Prentice-Hall 2009.
Notes	Notes for the practical sessions are available online. Each student is required to preview the corresponding notes before each practical session. Some prework is required and will be outlined in either the lecture or the laboratory materials

Required unit materials and/ or recommended readings	Required unit materials: Laboratory Notes (online) Recommended readings Floyd, Chapter 11, “Programmable Logic and Software”

Unit Schedule

Timetable

This is a tentative timetable and is subject to change during the Session. Please attend all lectures and practicals to ensure you do not miss out on important information.

Week	Lectures	Practicals
1	Outline Programmable Logic Devices Generic Array Logics (GALs)	
2	Shift Register Design Applications	Practical 1 – PLD Implementation of Shift Register Circuits
3	Counter Design and Applications Synchronous Cascadable Counters	Practical 2 – PLD Implementation of Synchronous Cascadable Counters
4	Finite State Machines (FSM) and Timing control of FSM Traffic Light Controllers	Practical 3 – Design and Implementation of a Traffic Light Controller, and Design and Implementation of MOD-n Counters with Single-Cycle Operation
5	Boundary Scan Testing	Practical 4 – Boundary Scan Testing with Signature Analysis
6	Review of Number Systems	Practical 5 – Boundary Scan Testing with Signature Analysis
7	Introduction to Group Project	Practical 6 – Traffic Light Controller Design and implementation (GAL – Team Project)
8	Product Minimisation and Glitch Free Operation	Practical 7 – Traffic Light Controller Design and implementation
9	Group Project Review	Practical 8 – Traffic Light Controller Design and implementation
10	Group Project Review	Practical 9 – Traffic Light Controller Design and implementation
11	Group Project Review	Practical 10 – Traffic Light Controller Design and implementation
12	Group Project Review	Practical 11 – Traffic Light Controller Design and implementation

13	Revision	Practical 12 – Revision

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central. Students should be aware of the following policies in particular with regard to Learning and Teaching:

Academic Honesty Policy http://mq.edu.au/policy/docs/academic_honesty/policy.html

Assessment Policy http://mq.edu.au/policy/docs/assessment/policy_2016.html

Grade Appeal Policy http://mq.edu.au/policy/docs/gradeappeal/policy.html

Complaint Management Procedure for Students and Members of the Public http://www.mq.edu.au/policy/docs/complaint_management/procedure.html

Disruption to Studies Policy (in effect until Dec 4th, 2017): http://www.mq.edu.au/policy/docs/disruption_studies/policy.html

Special Consideration Policy (in effect from Dec 4th, 2017): https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policies/special-consideration

In addition, a number of other policies can be found in the Learning and Teaching Category of Policy Central.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/support/student_conduct/

Results

Results shown in *iLearn*, or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au.

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise

- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Understand applications and performance capabilities of programmable logic devices
- Ability to apply logic design procedures to programmable logic devices, such as implementing finite state machines
- Ability to effectively manipulate designs of digital systems that have been implemented on programmable logic devices, based on different criteria
- Demonstrate engagement to active learning as well as self-learning capability in a group manner

Assessment tasks

- Diagnostic Quiz
- Practical 1 to 3 Report
- Design Assessment
- Final Report
- Engagement

- Exam

Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

Learning outcomes

- Ability to effectively manipulate designs of digital systems that have been implemented on programmable logic devices, based on different criteria
- Demonstrate engagement to active learning as well as self-learning capability in a group manner

Assessment tasks

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Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcomes

- Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays
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Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Understand key concepts, such as finite state machines, as well as their implementation on programmable logic arrays
- Understand applications and performance capabilities of programmable logic devices
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- Final Report
- Engagement
- Exam

Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

Learning outcomes

- Understand applications and performance capabilities of programmable logic devices
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Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Understand applications and performance capabilities of programmable logic devices
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Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcomes

- Ability to apply logic design procedures to programmable logic devices, such as implementing finite state machines
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Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

Learning outcome

- Demonstrate engagement to active learning as well as self-learning capability in a group

manner

Assessment tasks

- Diagnostic Quiz
- Engagement

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Learning outcome

- Demonstrate engagement to active learning as well as self-learning capability in a group manner

Assessment tasks

- Diagnostic Quiz
- Engagement