ELEC446

Advanced Computer Engineering

S1 Day 2014

Dept of Engineering

Contents

General Information

Unit convenor and teaching staff
Unit Convenor
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Credit points
3

Prerequisites
ELEC342(P) and ELEC343(P)

Corequisites

Co-badged status

Unit description
This unit integrates prior learning in a specialist area of engineering with problem solving, emerging technology and aspects of engineering application, technical reporting and self-management to prepare students to work at a professional capacity. The unit aims to address the application of fundamental principles and methods at an advanced level in the context of standards and practices, modelling, analysis, design and practical implementation. The unit also develops skills in the critical evaluation of information, software and sources of error, and experimental methods. Learning will be achieved using case studies, laboratories, presentations, group work and traditional lecture format. The specific topics will focus on current advances in the area such as FPGA design, digital microelectronics, digital arithmetics, and software CAD tools.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior

Understand the effect of parasitics and loading on CMOS circuit performance

Be able to design leaf cells for standard-cell and full-custom projects

Be able to estimate complementary CMOS circuit performance, size and noise margin

Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance

Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Assessment Tasks

Name	Weighting	Due
Practical 1	6%	13/03/2014
Practical 2	6%	27/03/2014
Practical 3	6%	10/04/2014
Practical 4	6%	15/05/2014
Practical 5	6%	29/05/2014
Report	10%	6/06/2014
Exam	60%	June

Practical 1

Due: **13/03/2014**
Weighting: **6%**

Schematics in ASIC Design using Electric Design Suite

On successful completion you will be able to:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior

Practical 2

Due: **27/03/2014**
Weighting: **6%**

Layouts in ASIC Design using Electric Design Suite

On successful completion you will be able to:

- Understand the effect of parasitics and loading on CMOS circuit performance

Practical 3

Due: **10/04/2014**
Weighting: **6%**

HSPICE Design using Synopsys tools

On successful completion you will be able to:

- Be able to design leaf cells for standard-cell and full-custom projects

Practical 4

Due: **15/05/2014**
Weighting: **6%**

Implementation of a Full Adder using Electric Design Suite

On successful completion you will be able to:

- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance

Practical 5

Due: **29/05/2014**
Weighting: **6%**

Implementation of a Carry Ripple Adder using Electric Design Suite

On successful completion you will be able to:

- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Report

Due: **6/06/2014**
Weighting: **10%**

ASIC Design of Computer Arithmetic Units

On successful completion you will be able to:

- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Exam

Due: **June**
Weighting: **60%**

3-hour Closed Book

On successful completion you will be able to:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior
- Understand the effect of parasitics and loading on CMOS circuit performance
- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Delivery and Resources

VHDL

Electric Design Suite

Synopsys HSPICE

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central. Students should be aware of the following policies in particular with regard to Learning and Teaching:

Academic Honesty Policy http://mq.edu.au/policy/docs/academic_honesty/policy.html

Assessment Policy http://mq.edu.au/policy/docs/assessment/policy.html

Grading Policy http://mq.edu.au/policy/docs/grading/policy.html

Grade Appeal Policy http://mq.edu.au/policy/docs/gradeappeal/policy.html

Grievance Management Policy http://mq.edu.au/policy/docs/grievance_management/policy.html

Disruption to Studies Policy http://www.mq.edu.au/policy/docs/disruption_studies/policy.html *The Disruption to Studies Policy is effective from March 3 2014 and replaces the Special Consideration Policy.*

In addition, a number of other policies can be found in the Learning and Teaching Category of Policy Central.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/support/student_conduct/

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

IT Help

For help with University computer systems and technology, visit http://informatics.mq.edu.au/help/.

When using the University's IT, you must adhere to the Acceptable Use Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin

Assessment tasks

- Practical 4
- Practical 5
- Report
- Exam

Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcomes

- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Assessment tasks

- Practical 4
- Report

Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge,

scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior
- Understand the effect of parasitics and loading on CMOS circuit performance
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Assessment tasks

- Practical 1
- Practical 2
- Report
- Exam

Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

Learning outcomes

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior
- Understand the effect of parasitics and loading on CMOS circuit performance
- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
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Assessment tasks

- Practical 3
- Practical 4
- Practical 5
- Report
- Exam

Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Assessment tasks

- Practical 4
- Practical 5
- Exam

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance
- Understand fundamental microelectronic datapath design, including variations of adders

and multipliers

Assessment tasks

- Practical 3
- Practical 4
- Practical 5
- Report
- Exam

Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcomes

- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers

Assessment task

- Report

Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

Learning outcomes

- Understand the effect of parasitics and loading on CMOS circuit performance
- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand the importance of system level considerations such as floor planning, power

dissipation, clock skew and micro-architecture to system performance

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Report

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Learning outcomes

- Understand the effect of parasitics and loading on CMOS circuit performance
- Be able to design leaf cells for standard-cell and full-custom projects
- Be able to estimate complementary CMOS circuit performance, size and noise margin
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 5