ELEC846

Advanced Computer Engineering

S2 Day 2018

Dept of Engineering

Contents

General Information	2
Learning Outcomes	2
General Assessment Information	3
Assessment Tasks	3
Delivery and Resources	6
Policies and Procedures	6
Graduate Capabilities	8

General Information

Unit convenor and teaching staff
Course Convener and Lecturer in Charge
Ediz Cetin
ediz.cetin@mq.edu.au
Contact via Email
44 Waterloo Road, Room: 117
Tuesday's 13:30 – 14:30 hrs and Wednesday's 13:00 – 14:00 hrs

Credit points
4

Prerequisites
Admission to MEng and ELEC643

Corequisites

Co-badged status
ELEC446, ELEC646

Unit description
This unit integrates prior learning in the specialist area of electronics engineering with problem solving, emerging technology and aspects of engineering application, technical reporting and self-management to prepare students to work at a professional capacity. The unit aims to address the application of fundamental principles and methods in computer engineering at an advanced level in the context of standards and practices, modelling, analysis, design and practical implementation. The unit also develops skills in the critical evaluation of information, software and sources of error, and experimental methods relevant to computer engineering. Learning will be achieved using case studies, laboratories, presentations, group work and traditional lecture format. The specific topics will focus on current advances in the area such as FPGA design, digital microelectronics, digital arithmetic, and software CAD tools.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on

circuit behavior.

Understand the effect of parasitics and loading on CMOS circuit performance.

Be able to design leaf cells for standard-cell and full-custom projects.

Be able to estimate complementary CMOS circuit performance, size and noise margin.

Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.

Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

General Assessment Information

Grading and passing requirement for unit

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD).

For further details about grading, please refer below in the policies and procedures section.

Late submissions and Resubmissions

Late submissions will attract a penalty of 10% marks per day. Extenuating circumstances will be considered upon lodgment of an application for special consideration.

Assessment Tasks

Name	Weighting	Hurdle	Due
Schematics in ASIC Design	8%	No	Week 2 and 3
Layouts in ASIC Design	8%	No	Week 4 and 5
HSPICE	8%	No	Week 6 and 7
Full Adder	8%	No	Week 9 and 10
Ripple Carry Adder	8%	No	Week 11 and 12
ASIC Design Report	10%	No	Week 13
Exam	50%	No	TBD

Schematics in ASIC Design

Due: **Week 2 and 3**
Weighting: **8%**

Design and test a schematic circuit for a logic gate. Complete and test a schematic circuit for a module in a larger system.

On successful completion you will be able to:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.

Layouts in ASIC Design

Due: **Week 4 and 5**
Weighting: **8%**

Design and test the layout for the logic gate that was assigned to you in Practical 1. Complete and test the layout for a module in a larger system.

On successful completion you will be able to:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.

HSPICE

Due: **Week 6 and 7**
Weighting: **8%**

Perform HSPICE simulations of logic circuits.

On successful completion you will be able to:

- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.

Full Adder

Due: **Week 9 and 10**
Weighting: **8%**

Design and test the schematic and layout circuit for a Full Adder (FA). We will use Electric for the design and HSPICE to measure the different characteristics of the circuit.

On successful completion you will be able to:

- Understand the effect of parasitics and loading on CMOS circuit performance.

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Ripple Carry Adder

Due: **Week 11 and 12**
Weighting: **8%**

Design and test the schematic and layout circuit for a 4-bit Ripple Carry Adder (RCA). The FA cell designed in Practical 4 will be used to construct the RCA. We will use Electric for the design of the circuit and HSPICE to measure the different characteristics of the circuit.

On successful completion you will be able to:

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

ASIC Design Report

Due: **Week 13**
Weighting: **10%**

Report on each student's customized adder design.

On successful completion you will be able to:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders

and multipliers.

Exam

Due: **TBD**
Weighting: **50%**

3 hour closed book exam.

On successful completion you will be able to:

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Delivery and Resources

Textbook: Neil Weste and David Harris, “CMOS VLSI Design”, Addison Wesley, 3rd edition (2004), or 4th edition, 2011.

Notes for the “practical” sessions will be handed out in each session.

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy
- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Grade Appeal Policy
- Complaint Management Procedure for Students and Members of the Public
- Special Consideration Policy *(**Note:** The Special Consideration Policy is effective from 4*

December 2017 and replaces the Disruption to Studies Policy.)

Undergraduate students seeking more policy resources can visit the Student Policy Gateway (https://students.mq.edu.au/support/study/student-policy-gateway). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

If you would like to see all the policies relevant to Learning and Teaching visit Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central).

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/study/getting-started/student-conduct

Results

Results shown in *iLearn*, or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au.

No extensions will be granted. Late tasks will be accepted up to 72* hours after the submission deadline. There will be a deduction of 20%* of the total available marks made from the total awarded mark for each 24 hour period or part thereof that the submission is late (for example, 25 hours late in submission – 40% penalty). This penalty does not apply for cases in which an application for special consideration is made and approved.

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

PG - Capable of Professional and Personal Judgment and Initiative

Our postgraduates will demonstrate a high standard of discernment and common sense in their professional and personal judgment. They will have the ability to make informed choices and decisions that reflect both the nature of their professional work and their personal perspectives.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.

Assessment tasks

- Layouts in ASIC Design
- HSPICE
- Full Adder
- Ripple Carry Adder
- ASIC Design Report
- Exam

PG - Discipline Knowledge and Skills

Our postgraduates will be able to demonstrate a significantly enhanced depth and breadth of knowledge, scholarly understanding, and specific subject content knowledge in their chosen fields.

This graduate capability is supported by:

Learning outcomes

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- Schematics in ASIC Design
- Layouts in ASIC Design
- HSPICE
- Full Adder
- Ripple Carry Adder
- ASIC Design Report
- Exam

PG - Critical, Analytical and Integrative Thinking

Our postgraduates will be capable of utilising and reflecting on prior knowledge and experience, of applying higher level critical thinking skills, and of integrating and synthesising learning and knowledge from a range of sources and environments. A characteristic of this form of thinking is the generation of new, professionally oriented knowledge through personal or group-based critique of practice and theory.

This graduate capability is supported by:

Learning outcomes

- Understand the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behavior.
- Understand the effect of parasitics and loading on CMOS circuit performance.
- Be able to design leaf cells for standard-cell and full-custom projects.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- Schematics in ASIC Design
- Layouts in ASIC Design
- HSPICE
- Full Adder
- Ripple Carry Adder
- ASIC Design Report
- Exam

PG - Research and Problem Solving Capability

Our postgraduates will be capable of systematic enquiry; able to use research skills to create new knowledge that can be applied to real world issues, or contribute to a field of study or practice to enhance society. They will be capable of creative questioning, problem finding and problem solving.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- Layouts in ASIC Design
- HSPICE
- Full Adder
- Ripple Carry Adder
- ASIC Design Report
- Exam

PG - Effective Communication

Our postgraduates will be able to communicate effectively and convey their views to different social, cultural, and professional audiences. They will be able to use a variety of technologically supported media to communicate with empathy using a range of written, spoken or visual formats.

This graduate capability is supported by:

Learning outcomes

- Be able to design leaf cells for standard-cell and full-custom projects.
- Be able to estimate complementary CMOS circuit performance, size and noise margin.
- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.
- Understand fundamental microelectronic datapath design, including variations of adders and multipliers.

Assessment tasks

- Layouts in ASIC Design
- HSPICE
- Full Adder
- Ripple Carry Adder
- ASIC Design Report
- Exam

PG - Engaged and Responsible, Active and Ethical Citizens

Our postgraduates will be ethically aware and capable of confident transformative action in relation to their professional responsibilities and the wider community. They will have a sense of connectedness with others and country and have a sense of mutual obligation. They will be able to appreciate the impact of their professional roles for social justice and inclusion related to national and global issues

This graduate capability is supported by:

Learning outcome

- Understand the importance of system level considerations such as floor planning, power dissipation, clock skew and micro-architecture to system performance.

Assessment tasks

- Full Adder
- Ripple Carry Adder
- ASIC Design Report
- Exam