ELEC343

Digital Systems Design

S2 Day 2014

Dept of Engineering

Contents

General Information

Unit convenor and teaching staff
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Credit points
3

Prerequisites
39cp including ELEC241(P)

Corequisites

Co-badged status

Unit description
This unit is a sequence of lectures and practical work on digital systems design, including: behavioural specification and description; architecture and structure design; software/ hardware co-design; technology mapping, verification and test. For greater complexity we choose Field-Programmable Gate Arrays (FPGAs) and a variety of software provided by the manufacturer (Xilinx), including Boolean equations, schematic entry, state machines, and a high-level design language (VHDL), itself supporting a variety of modes. This unit gives students the skills and knowledge needed to design modern digital systems.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL

Basic understanding of FPGA concepts and structures

Ability to use CAD software and implement basic digital logics on FPGAs

Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.

Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
Ability to work and communicate effectively within an integrated engineering team.
Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Assessment Tasks

Name	Weighting	Due
Practical 1	3%	Week 2
Practical 2	3%	Week 3
Practical 3	3%	Week 4
Practical 4	3%	Week 5
Report 1	3%	Week 6
Practical 5	2%	Week 6
Practical 6	2%	Week 7
Practical 7	2%	Week 9
Project 1 Deliverables	4%	Week 9
Practical 8	2%	Week 10
Practical 9	2%	Week 11
Practical 10	2%	Week 12
Practical 11	2%	Week 13
Project 2 Deliverables	4%	Week 13
Report 2	3%	Week 13
Exam	60%	Week 15

Practical 1

Due: **Week 2**
Weighting: **3%**

Schematic Capture and Hierarchical Design

On successful completion you will be able to:

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures
- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to work and communicate effectively within an integrated engineering team.

Practical 2

Due: **Week 3**
Weighting: **3%**

Getting Started with VHDL and Modelsim

On successful completion you will be able to:

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures
- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to work and communicate effectively within an integrated engineering team.

Practical 3

Due: **Week 4**
Weighting: **3%**

Basic VHDL Design Examples

On successful completion you will be able to:

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures
- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to work and communicate effectively within an integrated engineering team.

Practical 4

Due: **Week 5**
Weighting: **3%**

Basic VHDL Design Examples

On successful completion you will be able to:

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures
- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to work and communicate effectively within an integrated engineering team.

Report 1

Due: **Week 6**
Weighting: **3%**

Report on Practical 1 to 4

On successful completion you will be able to:

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures
- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to work and communicate effectively within an integrated engineering team.
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Practical 5

Due: **Week 6**
Weighting: **2%**

Team Project – Computer Design

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to work and communicate effectively within an integrated engineering team.

Practical 6

Due: **Week 7**
Weighting: **2%**

Team Project – Computer Design

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to work and communicate effectively within an integrated engineering team.

Practical 7

Due: **Week 9**
Weighting: **2%**

Team Project – Computer Design

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to work and communicate effectively within an integrated engineering team.

Project 1 Deliverables

Due: **Week 9**
Weighting: **4%**

Project 1 Deliverables

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to work and communicate effectively within an integrated engineering team.

Practical 8

Due: **Week 10**
Weighting: **2%**

Team Project – Traffic Light Controller Design and Implementation

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Practical 9

Due: **Week 11**
Weighting: **2%**

Team Project – Traffic Light Controller Design and Implementation

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Practical 10

Due: **Week 12**
Weighting: **2%**

Team Project – Traffic Light Controller Design and Implementation

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Practical 11

Due: **Week 13**
Weighting: **2%**

Team Project – Traffic Light Controller Design and Implementation

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Project 2 Deliverables

Due: **Week 13**
Weighting: **4%**

Project 2 Deliverables

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Report 2

Due: **Week 13**
Weighting: **3%**

Report 2 on Project 1 and 2

On successful completion you will be able to:

- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Exam

Due: **Week 15**
Weighting: **60%**

Exam (one 3-hour closed-book exam)

On successful completion you will be able to:

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures

- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Delivery and Resources

Lectures	There are two lectures per week. Lecture topics are provided in the (attached) timetable. From time to time, important announcements and notices will be made in the lectures. It is the responsibility of the student to be aware of these announcements and notices.
Assignments	None
Practical sessions	There are eleven practical sessions (each of three hours duration) starting in Week 2. Students will work in teams of two, and will attend one practical session each week. On the completion of each session, each group must complete and submit a “check-list” that itemizes each section of the practical. Each item is to be initialed by the group members on completion of the work. Your performance as recorded in your copies of the practical notes and summarized by your check-list will be used in the assessment of your practical work. Food and drink are not permitted in the laboratory. Students will not be permitted to enter the laboratory without appropriate footwear. Thongs and sandals are not acceptable.

Reports	Each team of two students will be required to submit two reports. One is based on the first four practicals and the other is based on the two team projects. **Reports should be submitted by the next Monday following the completion of the practical session of the report.**
What is required to complete the unit satisfactorily	Pass mark in each of the assessment components (practicals, reports, and examination)
Extension requests	Must be supported by evidence of medical conditions or misadventure.
Examination conditions	3-hour, closed book

Supplementary examination	Applications for a supplementary examination (based on medical reasons or misadventure) will only be considered if students have gained passes in the practicals and reports.
Grades and Final Mark	The grades of Credit, Distinction and High Distinction will be determined by setting “break-points” between Pass/Credit, Credit/Distinction and Distinction/High-Distinction. Linear interpolation will be used between break-points. Performance in all of the assessment components (practicals, reports, presentation and examination) will be used to set the break-points.
Text book	Charles, R. H. and John, L. K., “Digital Systems Design Using VHDL”, Second edition, Thompson, 2008
Reference book(s)	Vahid, F. and Lysecky, R., VHDL For Digital Design, Wiley 2007 Weste, N. and Harris, D., “CMOS VLSI Design -- A Circuit and Systems Perspecitive”, 3rd ed., (Addison-Wesley 2004) Andrew Rushton, “VHDL for Logic Synthesis (Second Edition)”, John Wiley and Sons, 2001
Notes	Notes for the practical sessions are available online. Each student is required to preview the corresponding notes before each practical session.

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central.

Students should be aware of the following policies in particular with regard to Learning and Teaching:

Academic Honesty Policy http://mq.edu.au/policy/docs/academic_honesty/policy.html

Assessment Policy http://mq.edu.au/policy/docs/assessment/policy.html

Grading Policy http://mq.edu.au/policy/docs/grading/policy.html

Grade Appeal Policy http://mq.edu.au/policy/docs/gradeappeal/policy.html

Grievance Management Policy http://mq.edu.au/policy/docs/grievance_management/policy.html

Disruption to Studies Policy http://www.mq.edu.au/policy/docs/disruption_studies/policy.html *The Disruption to Studies Policy is effective from March 3 2014 and replaces the Special Consideration Policy.*

In addition, a number of other policies can be found in the Learning and Teaching Category of Policy Central.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/support/student_conduct/

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

IT Help

For help with University computer systems and technology, visit http://informatics.mq.edu.au/help/.

When using the University's IT, you must adhere to the Acceptable Use Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

Learning outcomes

- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Assessment tasks

- Report 1
- Practical 5
- Practical 6
- Practical 7
- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables
- Report 2
- Exam

Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships

with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcomes

- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Assessment tasks

- Report 1
- Practical 5
- Practical 6
- Practical 7
- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables
- Report 2
- Exam

Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL

- Basic understanding of FPGA concepts and structures

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Report 1
- Project 1 Deliverables
- Project 2 Deliverables
- Report 2
- Exam

Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

Learning outcomes

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Report 1
- Project 1 Deliverables
- Project 2 Deliverables
- Report 2
- Exam

Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Basic understanding of VHDL concepts and syntax. Basic hardware programming using VHDL
- Basic understanding of FPGA concepts and structures
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Report 1
- Practical 5
- Practical 6
- Practical 7
- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables
- Report 2
- Exam

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We

want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.

Assessment tasks

- Practical 5
- Practical 6
- Practical 7
- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables
- Exam

Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcomes

- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Assessment tasks

- Practical 1
- Practical 2

- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables
- Exam

Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

Learning outcomes

- Ability to use CAD software and implement basic digital logics on FPGAs
- Ability to design a complex digital system using VHDL and implement it on FPGAs, such as a bus-structured computer or a traffic controller system.
- Knowledge of the characteristics of CMOS technology and the process of CMOS fabrication to a sufficient level to appreciate the implications of layout and technology on circuit behaviour.

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7

- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Learning outcomes

- Ability to follow Conceive-Design-Implement-Operate (CDIO) model in FPGA based digital systems construction.
- Ability to work and communicate effectively within an integrated engineering team.

Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Project 1 Deliverables
- Practical 8
- Practical 9
- Practical 10
- Practical 11
- Project 2 Deliverables