



ELEC8040

VLSI, Algorithms, and Systems

Session 2, Special circumstance 2020

School of Engineering

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Notice

As part of [Phase 3 of our return to campus plan](#), most units will now run tutorials, seminars and other small group learning activities on campus for the second half-year, while keeping an online version available for those students unable to return or those who choose to continue their studies online.

To check the availability of face-to-face and online activities for your unit, please go to [timetable viewer](#). To check detailed information on unit assessments visit your unit's iLearn space or consult your unit convenor.

General Information

Unit convenor and teaching staff
Unit Convener and Lecturer in Charge
Ediz Cetin
ediz.cetin@mq.edu.au
Contact via Contact via Email
44 Waterloo Road, Room: 117
Monday's 14:00 – 16:00 hrs.

Tutor
Felipe Barboza da Silva
felipe.barboza-da-silva@mq.edu.au
Contact via Contact via Email
44 Waterloo Road, Room:G05

Credit points
10

Prerequisites
Admission to MEngElecEng and 30cp at 3000 level or above

Corequisites

Co-badged status

Unit description
This unit looks at VLSI technology from the perspective of an enabling platform for digital, analog, and complete system solutions. By taking a systems approach driven by the applications and algorithms, the VLSI design is driven toward a more optimised solution by analysis at higher levels.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at <https://www.mq.edu.au/study/calendar-of-dates>

Learning Outcomes

On successful completion of this unit, you will be able to:

ULO1: Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.

ULO2: Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.

ULO3: Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.

ULO4: Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

ULO5: Execute a project to implement an application or VLSI algorithm and produce requirements, specifications, and designs for low-power, area and/or high performance.

General Assessment Information

Grading and passing requirement for unit

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/CR/D/HD).

For further details about grading, please refer below in the policies and procedures section.

Hurdle Requirements

There are no hurdle requirements.

Late submissions and Resubmissions

Late submissions will attract a penalty of 10% marks per day. Extenuating circumstances will be considered upon lodgment of a formal notice of disruption of studies.

Once an assignment submission has closed no resubmission of assignments will be permitted.

Assessment Tasks

Name	Weighting	Hurdle	Due
<u>Assignment 1</u>	10%	No	Week 4
<u>Project Report</u>	20%	No	Week 13
<u>Project Defence</u>	30%	No	Exam Period
<u>Assignment 2</u>	10%	No	Week 7
<u>Assignment 2 Defence</u>	15%	No	Week 7
<u>Assignment 1 Defence</u>	15%	No	Week 4

Assignment 1

Assessment Type ¹: Report

Indicative Time on Task ²: 15 hours

Due: **Week 4**

Weighting: **10%**

Assignment 1 Report (1000-word equivalent)

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

Project Report

Assessment Type ¹: Report

Indicative Time on Task ²: 35 hours

Due: **Week 13**

Weighting: **20%**

Project Report (2000-word equivalent)

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.
- Execute a project to implement an application or VLSI algorithm and produce requirements, specifications, and designs for low-power, area and/or high performance.

Project Defence

Assessment Type ¹: Viva/oral examination

Indicative Time on Task ²: 10 hours

Due: **Exam Period**

Weighting: **30%**

Project Defence

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.
- Execute a project to implement an application or VLSI algorithm and produce requirements, specifications, and designs for low-power, area and/or high performance.

Assignment 2

Assessment Type ¹: Report

Indicative Time on Task ²: 15 hours

Due: **Week 7**

Weighting: **10%**

Assignment 2 Report (1000-word equivalent)

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

Assignment 2 Defence

Assessment Type ¹: Viva/oral examination

Indicative Time on Task ²: 5 hours

Due: **Week 7**

Weighting: **15%**

Assignment 2 Defence

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

Assignment 1 Defence

Assessment Type ¹: Viva/oral examination

Indicative Time on Task ²: 5 hours

Due: **Week 4**

Weighting: **15%**

Assignment 1 Defence

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

¹ If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- the [Writing Centre](#) for academic skills support.

² Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation

Delivery and Resources

Textbook: None required to purchase. Lecturer will provide the reading material.

Suggested references: Keshab K. Parhi, “VLSI Digital Signal Processing Systems: Design and Implementation”, Wiley, 1998.

Policies and Procedures

Macquarie University policies and procedures are accessible from [Policy Central \(https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central\)](https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- [Academic Appeals Policy](#)
- [Academic Integrity Policy](#)
- [Academic Progression Policy](#)
- [Assessment Policy](#)
- [Fitness to Practice Procedure](#)
- [Grade Appeal Policy](#)
- [Complaint Management Procedure for Students and Members of the Public](#)
- [Special Consideration Policy](#) (**Note:** *The Special Consideration Policy is effective from 4 December 2017 and replaces the Disruption to Studies Policy.*)

Students seeking more policy resources can visit the [Student Policy Gateway \(https://students.mq.edu.au/support/study/student-policy-gateway\)](https://students.mq.edu.au/support/study/student-policy-gateway). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

If you would like to see all the policies relevant to Learning and Teaching visit [Policy Central \(https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central\)](https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central).

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: <https://students.mq.edu.au/study/getting-started/student-conduct>

Results

Results published on platform other than [eStudent](#), (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the

University. Once approved, final results will be sent to your student email address and will be made available in [eStudent](#). For more information visit ask.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Student Support

Macquarie University provides a range of support services for students. For details, visit <http://students.mq.edu.au/support/>

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to help you improve your marks and take control of your study.

- [Getting help with your assignment](#)
- [Workshops](#)
- [StudyWise](#)
- [Academic Integrity Module](#)

The Library provides online and face to face support to help you find and use relevant information resources.

- [Subject and Research Guides](#)
- [Ask a Librarian](#)

Student Services and Support

Students with a disability are encouraged to contact the [Disability Service](#) who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

If you are a Global MBA student contact globalmba.support@mq.edu.au

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the [Acceptable Use of IT Resources Policy](#). The policy applies to all who connect to the MQ network including students.

Changes from Previous Offering

Minor updates and re-structuring of the content.