ELEC2042

Digital Circuits and Systems

Session 2, Weekday attendance, North Ryde 2021

School of Engineering

Contents

Session 2 Learning and Teaching Update

The decision has been made to conduct study online for the remainder of Session 2 for all units WITHOUT mandatory on-campus learning activities. Exams for Session 2 will also be online where possible to do so.

This is due to the extension of the lockdown orders and to provide certainty around arrangements for the remainder of Session 2. We hope to return to campus beyond Session 2 as soon as it is safe and appropriate to do so.

Some classes/teaching activities cannot be moved online and must be taught on campus. You should already know if you are in one of these classes/teaching activities and your unit convenor will provide you with more information via iLearn. If you want to confirm, see the list of units with mandatory on-campus classes/teaching activities.

Visit the MQ COVID-19 information page for more detail.

General Information

Unit convenor and teaching staff
Convenor
Rex Di Bona
rex.dibona@mq.edu.au
Contact via via email
50 Waterloo Road
Friday 9-12am

Convenor
Alan Kan
alan.kan@mq.edu.au
Contact via via email
50 Waterloo Road
By Arrangement

Alan Kan
alan.kan@mq.edu.au

Credit points
10

Prerequisites
COMP115 or COMP1000

Corequisites

Co-badged status

Unit description
This unit aims to provide students with an understanding of, and fluency in, combinational and sequential logic design techniques commonly used in the design of large-scale digital systems, as well as exposure to hardware description languages. Students will apply this knowledge to the design and implementation of digital circuits and systems at the gate level, and also program field programmable gate arrays.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

ULO1: Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.

ULO2: Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

ULO3: Design fast and efficient combinatorial logic circuits at the gate level.

ULO4: Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA

ULO5: Describe the principle and operation of field programmable gate arrays (FPGAs)

General Assessment Information

Grading and passing requirement for unit

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD).

For further details about grading, please refer below in the policies and procedures section.

If you receive special consideration for the final exam, a supplementary exam will be scheduled in the supplementary examination period, typically about 3 to 4 weeks after the normal exam period. By making a special consideration application for the final exam you are declaring yourself available for a resit during the supplementary examination period and will not be eligible for a second special consideration approval based on pre-existing commitments. Please ensure you are familiar with the policy prior to submitting an application. Approved applicants will receive an individual notification one week prior to the exam with the exact date and time of their supplementary examination.

Hurdle Requirements

There are two hurdle requirements for passing this unit. The final examination is a hurdle requirement. A grade of 50% or more in the final examination is a condition of passing this unit. If you are given a second opportunity to sit the final examination as a result of failing to meet the minimum mark required, you will be offered that chance during the supplementary examination period and will be notified of the exact day and time after the publication of final results for the unit. The second attempt at a hurdle assessment is graded as pass fail. The maximum grade for a second attempt is the hurdle threshold grade.

Participation in practical sessions is a hurdle requirement and students are required to participate in at least 10/13 practical sessions to pass this unit

Late submissions and Resubmissions

Late submissions will attract a penalty of 20 marks per day. Extenuating circumstances will be considered upon lodgement of a formal notice of request for Special Consideration.

Resubmissions of work is not allowed.

Assessment Tasks

Name	Weighting	Hurdle	Due
Final Exam	50%	Yes	During Exam Period
Simple Design Task	10%	No	Week 7
Student Engagement	10%	Yes	Each Week
Complex Design Task	30%	No	Week 13

Final Exam

Assessment Type [1]: Examination
Indicative Time on Task [2]: 19 hours
Due: **During Exam Period**
Weighting: **50%**
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

There is a formal examination of the material covered in the pre-work, laboratory work, and lecture material presented during the unit. This is a hurdle assessment. You must pass the exam to be eligible to pass the unit. The exam is scheduled to last three hours.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Design fast and efficient combinatorial logic circuits at the gate level.
- Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA
- Describe the principle and operation of field programmable gate arrays (FPGAs)

Simple Design Task

Assessment Type [1]: Design Task
Indicative Time on Task [2]: 10 hours
Due: **Week 7**

Weighting: **10%**

This is the first design assignment. You will take the knowledge about digital circuits presented so far and design a circuit to perform a given task.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

Student Engagement

Assessment Type [1]: Log book
Indicative Time on Task [2]: 12 hours
Due: **Each Week**
Weighting: **10%**
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

Students are expected to actively participate in the learning activities with a developing level of independence. Before each practical session students may be required to complete preparatory work in a log book. During the practical sessions students must also complete their work and keep a log book of their work.

In pure online versions of the class the work will be conducted using a simulator and the results will need to be submitted for assessment each week.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Design fast and efficient combinatorial logic circuits at the gate level.
- Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA

Complex Design Task

Assessment Type [1]: Design Task
Indicative Time on Task [2]: 20 hours
Due: **Week 13**
Weighting: **30%**

This assignment is a design assignment. You must design and present a state machine to solve the project outline given. A rubric will be issued to indicate what is being looked for in the assignment.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Design fast and efficient combinatorial logic circuits at the gate level.
- Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA

---

[1] If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- the Writing Centre for academic skills support.

[2] Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation

Delivery and Resources

This is a hands on unit, centred about physical circuits. We will be using physical trainer boards to build digital circuits and experiment with those circuits. All students are expected to attend their practical session on Campus.

The text book is an electronics book, available free of charge to all students through the library.

https://learning.oreilly.com/library/view/digital-electronics-principles/9780470032145/

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://policie

s.mq.edu.au). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy
- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Grade Appeal Policy
- Complaint Management Procedure for Students and Members of the Public
- Special Consideration Policy

Students seeking more policy resources can visit Student Policies (https://students.mq.edu.au/support/study/policies). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit Policy Central (https://policies.mq.edu.au) and use the search tool.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/admin/other-resources/student-conduct

Results

Results published on platform other than eStudent, (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to help you improve your marks and take control of your study.

- Getting help with your assignment
- Workshops
- StudyWise
- Academic Integrity Module

The Library provides online and face to face support to help you find and use relevant

information resources.

- Subject and Research Guides
- Ask a Librarian

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

If you are a Global MBA student contact globalmba.support@mq.edu.au

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Changes from Previous Offering

in this offering the programmable GAL hardware component is replaced by FPGAs as the modern replacement.