



# ELEC8870

## High Performance IC Design

Session 2, In person-scheduled-weekday, North Ryde 2022

*School of Engineering*

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## General Information

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Credit points

10

Prerequisites

Admission to MEngElecEng and 30cp at 3000 level or above

Corequisites

Co-badged status

Unit description

From modern telecommunications to tablet computing and from mobile handsets to the cloud, the limits of integrated circuit technology are being pushed to the limits of what is possible in terms of speed, size, and power. Beyond the IC itself, packaging concerns, both electrical and thermal, provide additional constraints in the design of the modern high performance integrated circuit. This unit will be taught from the research of both resident and visiting staff as well as from the latest research around the world.

## Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at <https://www.mq.edu.au/study/calendar-of-dates>

## Learning Outcomes

On successful completion of this unit, you will be able to:

**ULO1:** Develop an understanding of different semiconductor technologies

**ULO2:** Develop proficiency in using standard electronic design automation (EDA) tools for IC design

**ULO3:** Perform integrated circuit (IC) design in a commercially used semiconductor

technology

**ULO4:** Develop an understanding of the technical concept required for implementing various high frequency on-chip active and passive circuits

**ULO5:** Demonstrate self-learning, time-management, technical report writing, project management (individually and as a group)

## General Assessment Information

In order to pass this unit a student must obtain a mark of 50 or more overall to obtain a passing grade P/ CR/ D/ HD.

The submission of lab reports and assignments will be done via iLearn. For any late submissions please see the Late Assessment Submission policy below.

If you receive special consideration for the final exam, a supplementary exam will be scheduled by the faculty during a supplementary exam period, typically about 3 to 4 weeks after the normal exam period. By making a special consideration application for the final exam you are declaring yourself available for a resit during the supplementary examination period and will not be eligible for a second special consideration approval based on pre-existing commitments. Please ensure you are familiar with the policy prior to submitting an application. Approved applicants will receive an individual notification one week prior to the exam with the exact date and time of their supplementary examination.

Final project presentation will be in Week 13 during laboratory hours.

### Late Assessment Submission Penalty

From 1 July 2022, Students enrolled in Session based units with written assessments will have the following university standard late penalty applied. Please see <https://students.mq.edu.au/study/assessment-exams/assessments> for more information.

Unless a Special Consideration request has been submitted and approved, a 5% penalty (of the total possible mark) will be applied each day a written assessment is not submitted, up until the 7<sup>th</sup> day (including weekends). After the 7<sup>th</sup> day, a grade of '0' will be awarded even if the assessment is submitted. Submission time for all written assessments is set at **11:55 pm**. A 1-hour grace period is provided to students who experience a technical concern.

For any late submission of time-sensitive tasks, such as scheduled tests/exams, performance assessments/presentations, and/or scheduled practical assessments/labs, students need to submit an application for Special Consideration.

### Assessments where Late Submissions will be accepted

In this unit, late submissions will be accepted as follows:

- Assignment - YES, Standard late penalty applies
- Lab Report - YES, Standard late penalty applies

- Lab Participation - NO, unless Special Consideration is granted
- Design Presentation - NO, unless Special Consideration is granted
- Final Examination - NO, unless Special Consideration is granted

## Assessment Tasks

| Name                                | Weighting | Hurdle | Due                     |
|-------------------------------------|-----------|--------|-------------------------|
| <a href="#">Final examination</a>   | 50%       | No     | Exam period             |
| <a href="#">Lab report</a>          | 15%       | No     | Week 4, Week 8, Week 13 |
| <a href="#">Assignment</a>          | 15%       | No     | Week 3, Week 6          |
| <a href="#">Lab participation</a>   | 5%        | No     | Weekly lab              |
| <a href="#">Design Presentation</a> | 15%       | No     | Week 13                 |

### Final examination

Assessment Type <sup>1</sup>: Examination

Indicative Time on Task <sup>2</sup>: 49 hours

Due: **Exam period**

Weighting: **50%**

Final examination held in the formal exam period.

On successful completion you will be able to:

- Develop an understanding of different semiconductor technologies
- Develop an understanding of the technical concept required for implementing various high frequency on-chip active and passive circuits
- Demonstrate self-learning, time-management, technical report writing, project management (individually and as a group)

### Lab report

Assessment Type <sup>1</sup>: Lab report

Indicative Time on Task <sup>2</sup>: 12 hours

Due: **Week 4, Week 8, Week 13**

Weighting: **15%**

Three lab reports on design works

On successful completion you will be able to:

- Develop proficiency in using standard electronic design automation (EDA) tools for IC design
- Perform integrated circuit (IC) design in a commercially used semiconductor technology
- Develop an understanding of the technical concept required for implementing various high frequency on-chip active and passive circuits
- Demonstrate self-learning, time-management, technical report writing, project management (individually and as a group)

## Assignment

Assessment Type <sup>1</sup>: Problem set

Indicative Time on Task <sup>2</sup>: 12 hours

Due: **Week 3, Week 6**

Weighting: **15%**

Assignments based on lecture material

On successful completion you will be able to:

- Develop an understanding of different semiconductor technologies
- Develop proficiency in using standard electronic design automation (EDA) tools for IC design
- Perform integrated circuit (IC) design in a commercially used semiconductor technology
- Develop an understanding of the technical concept required for implementing various high frequency on-chip active and passive circuits

## Lab participation

Assessment Type <sup>1</sup>: Design Task

Indicative Time on Task <sup>2</sup>: 0 hours

Due: **Weekly lab**

Weighting: **5%**

Active and passive circuit implementation in the practical activities. Participation workload is assumed to take place inside the schedule teaching activity.

On successful completion you will be able to:

- Develop proficiency in using standard electronic design automation (EDA) tools for IC design
- Perform integrated circuit (IC) design in a commercially used semiconductor technology
- Demonstrate self-learning, time-management, technical report writing, project management (individually and as a group)

## Design Presentation

Assessment Type <sup>1</sup>: Presentation

Indicative Time on Task <sup>2</sup>: 12 hours

Due: **Week 13**

Weighting: **15%**

Powerpoint or other suitable format presentation on the final design task.

On successful completion you will be able to:

- Develop proficiency in using standard electronic design automation (EDA) tools for IC design
- Perform integrated circuit (IC) design in a commercially used semiconductor technology
- Develop an understanding of the technical concept required for implementing various high frequency on-chip active and passive circuits
- Demonstrate self-learning, time-management, technical report writing, project management (individually and as a group)

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<sup>1</sup> If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- the [Writing Centre](#) for academic skills support.

<sup>2</sup> Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation

## Delivery and Resources

Industry standard CAD tool Microwave Office will be used for design project and laboratory

exercises. Students will be provided with details on how to access this tool.

## Unit Schedule

Refer to iLearn and lecture notes for the lecture schedule.

There will be practical during week-1. The first week laboratory will get students oriented to the CAD tool which will be used in this unit.

## Policies and Procedures

Macquarie University policies and procedures are accessible from [Policy Central \(https://policies.mq.edu.au\)](https://policies.mq.edu.au). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- [Academic Appeals Policy](#)
- [Academic Integrity Policy](#)
- [Academic Progression Policy](#)
- [Assessment Policy](#)
- [Fitness to Practice Procedure](#)
- [Assessment Procedure](#)
- [Complaints Resolution Procedure for Students and Members of the Public](#)
- [Special Consideration Policy](#)

Students seeking more policy resources can visit [Student Policies \(https://students.mq.edu.au/support/study/policies\)](https://students.mq.edu.au/support/study/policies). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit [Policy Central \(https://policies.mq.edu.au\)](https://policies.mq.edu.au) and use the [search tool](#).

## Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: <https://students.mq.edu.au/admin/other-resources/student-conduct>

## Results

Results published on platform other than [eStudent](#), (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in [eStudent](#). For more information visit [ask.mq.edu.au](https://ask.mq.edu.au) or if you are a Global MBA student contact [globalmba.support@mq.edu.au](mailto:globalmba.support@mq.edu.au)

## Academic Integrity

At Macquarie, we believe [academic integrity](#) – honesty, respect, trust, responsibility, fairness and courage – is at the core of learning, teaching and research. We recognise that meeting the expectations required to complete your assessments can be challenging. So, we offer you a

range of resources and services to help you reach your potential, including free [online writing and maths support](#), [academic skills development](#) and [wellbeing consultations](#).

## Student Support

Macquarie University provides a range of support services for students. For details, visit <http://students.mq.edu.au/support/>

### The Writing Centre

[The Writing Centre](#) provides resources to develop your English language proficiency, academic writing, and communication skills.

- [Workshops](#)
- [Chat with a WriteWISE peer writing leader](#)
- [Access StudyWISE](#)
- [Upload an assignment to Studiosity](#)
- [Complete the Academic Integrity Module](#)

The Library provides online and face to face support to help you find and use relevant information resources.

- [Subject and Research Guides](#)
- [Ask a Librarian](#)

## Student Services and Support

Macquarie University offers a range of [Student Support Services](#) including:

- [IT Support](#)
- [Accessibility and disability support](#) with study
- Mental health [support](#)
- [Safety support](#) to respond to bullying, harassment, sexual harassment and sexual assault
- [Social support including information about finances, tenancy and legal issues](#)

## Student Enquiries

Got a question? Ask us via [AskMQ](#), or contact [Service Connect](#).

## IT Help

For help with University computer systems and technology, visit [http://www.mq.edu.au/about\\_us/offices\\_and\\_units/information\\_technology/help/](http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/).

When using the University's IT, you must adhere to the [Acceptable Use of IT Resources Policy](#). The policy applies to all who connect to the MQ network including students.



## Changes from Previous Offering

No changes have been made to the delivery of the unit based on previous feedback.

## ALTUM RF BEST STUDENT PRIZE

ALTUM RF (<https://www.altumrf.com/>) will award the top student of this unit during week 13 final project presentation session.

The top student is the student with highest marks in the unit by week 13. Final exam marks are not included for Altum RF award.

The award amount is \$250. The award may be shared between multiple students in the event equal top marks.