General Information

Unit convenor and teaching staff
Unit Convener and Lecturer in Charge
Ediz Cetin
ediz.cetin@mq.edu.au

Contact via Email
44 Waterloo Road, Room: 117
Monday’s 14:00 – 16:00 hrs.

Credit points
10

Prerequisites
Admission to MEngElecEng and 30cp at 3000 level or above

Corequisites

Co-badged status

Unit description
This unit looks at VLSI technology from the perspective of an enabling platform for digital, analog, and complete system solutions. By taking a systems approach driven by the applications and algorithms, the VLSI design is driven toward a more optimised solution by analysis at higher levels.

Important Academic Dates
Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes
On successful completion of this unit, you will be able to:

ULO1: Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.

ULO2: Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.

ULO3: Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.

ULO4: Demonstrate competency in the practical use of standard VLSI work products for
communication and documentation of engineering processes.

**ULO5:** Execute a project to implement an application or VLSI algorithm and produce requirements, specifications, and designs for low-power, area and/or high performance.

**General Assessment Information**

**Grading and passing requirement for unit**

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/CR/D/HD).

For further details about grading, please refer below in the policies and procedures section.

**Hurdle Requirements**

There are no hurdle requirements.

**Late Assessment Submission Penalty**

From 1 July 2022, Students enrolled in Session based units with written assessments will have the following university standard late penalty applied. Please see [https://students.mq.edu.au/study/assessment-exams/assessments](https://students.mq.edu.au/study/assessment-exams/assessments) for more information.

Unless a Special Consideration request has been submitted and approved, a 5% penalty (of the total possible mark) will be applied each day a written assessment is not submitted, up until the 7th day (including weekends). After the 7th day, a grade of '0' will be awarded even if the assessment is submitted. Submission time for all written assessments is set at **11:55 pm**. A 1-hour grace period is provided to students who experience a technical concern.

For any late submission of time-sensitive tasks, such as scheduled tests/exams, performance assessments/presentations, and/or scheduled practical assessments/labs, students need to submit an application for **Special Consideration**.

**Assessments where Late Submissions will be accepted**

In this unit, late submissions will accepted as follows:

Assignment 1 report, Assignment 2 report and Project Report – YES, Standard Late Penalty applies

<table>
<thead>
<tr>
<th>Name</th>
<th>Weighting</th>
<th>Hurdle</th>
<th>Due</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assignment 1</td>
<td>10%</td>
<td>No</td>
<td>Week 4</td>
</tr>
<tr>
<td>Assignment 1 Defence</td>
<td>15%</td>
<td>No</td>
<td>Week 4</td>
</tr>
<tr>
<td>Assignment 2</td>
<td>10%</td>
<td>No</td>
<td>Week 7</td>
</tr>
<tr>
<td>Assignment 2 Defence</td>
<td>15%</td>
<td>No</td>
<td>Week 7</td>
</tr>
<tr>
<td>Name</td>
<td>Weighting</td>
<td>Hurdle</td>
<td>Due</td>
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</tr>
<tr>
<td>Project Report</td>
<td>20%</td>
<td>No</td>
<td>Week 13</td>
</tr>
<tr>
<td>Project Defence</td>
<td>30%</td>
<td>No</td>
<td>Exam Period</td>
</tr>
</tbody>
</table>

### Assignment 1

**Assessment Type**: Report  
**Indicative Time on Task**: 15 hours  
**Due**: Week 4  
**Weighting**: 10%

Assignment 1 Report (1000-word equivalent)

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

### Assignment 1 Defence

**Assessment Type**: Viva/oral examination  
**Indicative Time on Task**: 5 hours  
**Due**: Week 4  
**Weighting**: 15%

Assignment 1 Defence

On successful completion you will be able to:

- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
• Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
• Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
• Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

Assignment 2
Assessment Type 1: Report
Indicative Time on Task 2: 15 hours
Due: Week 7
Weighting: 10%

Assignment 2 Report (1000-word equivalent)

On successful completion you will be able to:
• Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
• Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
• Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
• Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

Assignment 2 Defence
Assessment Type 1: Viva/oral examination
Indicative Time on Task 2: 5 hours
Due: Week 7
Weighting: 15%

Assignment 2 Defence

On successful completion you will be able to:
• Demonstrate an understanding of foundational impact of implementation technology and
develop advanced VLSI engineering skills.

- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.

Project Report

Assessment Type 1: Report
Indicative Time on Task 2: 35 hours
Due: Week 13
Weighting: 20%

Project Report (2000-word equivalent)

On successful completion you will be able to:
- Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
- Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
- Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
- Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.
- Execute a project to implement an application or VLSI algorithm and produce requirements, specifications, and designs for low-power, area and/or high performance.

Project Defence

Assessment Type 1: Viva/oral examination
Indicative Time on Task 2: 10 hours
Due: Exam Period
Weighting: 30%
On successful completion you will be able to:

• Demonstrate an understanding of foundational impact of implementation technology and develop advanced VLSI engineering skills.
• Evaluate systems and algorithms in regard to their implementation as VLSI integrated circuits.
• Incorporate design trade-offs involving area, power and performance as a result of algorithm and architecture selection for practical problems requiring VLSI solutions.
• Demonstrate competency in the practical use of standard VLSI work products for communication and documentation of engineering processes.
• Execute a project to implement an application or VLSI algorithm and produce requirements, specifications, and designs for low-power, area and/or high performance.

1 If you need help with your assignment, please contact:

• the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
• the Writing Centre for academic skills support.

2 Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation

Delivery and Resources

Textbook: None required to purchase. Lecturer will provide the reading material.


Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://policies.mq.edu.au). Students should be aware of the following policies in particular with regard to Learning and Teaching:

• Academic Appeals Policy
• Academic Integrity Policy
• Academic Progression Policy
• Assessment Policy
• Fitness to Practice Procedure
• Assessment Procedure
• Complaints Resolution Procedure for Students and Members of the Public
• **Special Consideration Policy**

Students seeking more policy resources can visit [Student Policies](https://students.mq.edu.au/support/study/policies). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit [Policy Central](https://policies.mq.edu.au) and use the search tool.

**Student Code of Conduct**

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: [https://students.mq.edu.au/admin/other-resources/student-conduct](https://students.mq.edu.au/admin/other-resources/student-conduct)

**Results**

Results published on platform other than eStudent, (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit [ask.mq.edu.au](http://ask.mq.edu.au) or if you are a Global MBA student contact [globalmba.support@mq.edu.au](mailto:globalmba.support@mq.edu.au)

**Academic Integrity**

At Macquarie, we believe academic integrity – honesty, respect, trust, responsibility, fairness and courage – is at the core of learning, teaching and research. We recognise that meeting the expectations required to complete your assessments can be challenging. So, we offer you a range of resources and services to help you reach your potential, including free online writing and maths support, academic skills development and wellbeing consultations.

**Student Support**

Macquarie University provides a range of support services for students. For details, visit [http://students.mq.edu.au/support/](http://students.mq.edu.au/support/)

**The Writing Centre**

The Writing Centre provides resources to develop your English language proficiency, academic writing, and communication skills.

- Workshops
- Chat with a WriteWISE peer writing leader
- Access StudyWISE
- Upload an assignment to Studiosity
- Complete the Academic Integrity Module

The Library provides online and face to face support to help you find and use relevant information resources.

- Subject and Research Guides
Macquarie University offers a range of **Student Support Services** including:

- **IT Support**
- **Accessibility and disability support** with study
- **Mental health support**
- **Safety support** to respond to bullying, harassment, sexual harassment and sexual assault
- **Social support including information about finances, tenancy and legal issues**

**Student Enquiries**

Got a question? Ask us via AskMQ, or contact Service Connect.

**IT Help**

For help with University computer systems and technology, visit [http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/](http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/).

When using the University's IT, you must adhere to the [Acceptable Use of IT Resources Policy](http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/). The policy applies to all who connect to the MQ network including students.

**Changes from Previous Offering**

Minor updates to the content.

### Engineers Australia Competency Mapping

<table>
<thead>
<tr>
<th>EA Competency Standard</th>
<th>Unit Learning Outcomes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Knowledge and Skill Base</td>
<td>Unit Learning Outcomes</td>
</tr>
<tr>
<td>1.1 Comprehensive, theory-based understanding of the underpinning fundamentals applicable to the engineering discipline.</td>
<td>ULO1</td>
</tr>
<tr>
<td>1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing.</td>
<td></td>
</tr>
<tr>
<td>1.3 In-depth understanding of specialist bodies of knowledge</td>
<td>ULO1, ULO3</td>
</tr>
<tr>
<td>1.4 Discernment of knowledge development and research directions</td>
<td></td>
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<tr>
<td>1.5 Knowledge of engineering design practice</td>
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<tr>
<td>1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice.</td>
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</tbody>
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[https://unitguides.mq.edu.au/unit_offerings/149822/unit_guide/print](https://unitguides.mq.edu.au/unit_offerings/149822/unit_guide/print)
### Engineering Application Ability

<table>
<thead>
<tr>
<th>2.1 Application of established engineering methods to complex problem solving</th>
<th>ULO2</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2 Fluent application of engineering techniques, tools and resources.</td>
<td>ULO2, ULO3, ULO4, ULO5</td>
</tr>
<tr>
<td>2.3 Application of systematic engineering synthesis and design processes.</td>
<td>ULO2, ULO4</td>
</tr>
<tr>
<td>2.4 Application of systematic approaches to the conduct and management of engineering projects.</td>
<td>ULO4, ULO5</td>
</tr>
</tbody>
</table>

### Professional and Personal Attributes

<table>
<thead>
<tr>
<th>3.1 Ethical conduct and professional accountability.</th>
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<tbody>
<tr>
<td>3.2 Effective oral and written communication in professional and lay domains.</td>
</tr>
<tr>
<td>3.3 Creative, innovative and pro-active demeanour.</td>
</tr>
<tr>
<td>3.4 Professional use and management of information.</td>
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<tr>
<td>3.5 Orderly management of self, and professional conduct.</td>
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<tr>
<td>3.6 Effective team membership and team leadership</td>
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