ELEC2042

Digital Circuits and Systems

Session 2, In person-scheduled-weekday, North Ryde 2023

School of Engineering

Contents

General Information

Unit convenor and teaching staff
Unit Co-convenor
Rex Di Bona
rex.dibona@mq.edu.au
Contact via Private message on iLearn
50 Waterloo Road
By Appointment

Unit Co-convenor
Alan Kan
alan.kan@mq.edu.au
Contact via Private message on iLearn
Mon 10-11 am, Confirm location via private message prior

Credit points
10

Prerequisites
COMP115 or COMP1000

Corequisites

Co-badged status

Unit description
This unit aims to provide students with an understanding of, and fluency in, combinational and sequential logic design techniques commonly used in the design of large-scale digital systems, as well as exposure to hardware description languages. Students will apply this knowledge to the design and implementation of digital circuits and systems at the gate level, and also program field programmable gate arrays.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

ULO1: Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.

ULO2: Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

ULO3: Design fast and efficient combinatorial logic circuits at the gate level.

ULO4: Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA

ULO5: Describe the principle and operation of field programmable gate arrays (FPGAs)

General Assessment Information

Grading and passing requirement for unit

There are three quizzes, one minor project and one complex design task for this unit. Quizzes will be conducted on iLearn. Assessment of the minor project is through a report. Assessment of the complex design task is through a written report and code.

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD) and pass the hurdle requirements.

For further details about grading, please refer below in the policies and procedures section.

Hurdle Requirements

Quiz 2 and the complex design task have a hurdle requirement. Achieving a grade of 50% or more is required in these tasks as a condition of passing this unit. If you do not pass the hurdle requirement for Quiz 2, you may be given a second attempt if you demonstrated that you made a reasonable first attempt. If you do not pass the hurdle requirement for the complex design task on the first attempt, you may be offered a supplementary task if giving a second attempt and passing the complex design task will allow you to pass the unit. All second attempts at the hurdle assessment will be graded as pass/fail. **The maximum grade for a second attempt is the hurdle threshold grade**.

Late submissions and Resubmissions

Resubmission of work is not allowed.

Unless a Special Consideration request has been submitted and approved, a 5% penalty (of the total possible mark of the task) will be applied for each day a written report or presentation assessment is not submitted, up until the 7th day (including weekends). After the 7th day, a grade of ‘0’ will be awarded even if the assessment is submitted. The submission time for all uploaded assessments is 11:55 pm. A 1-hour grace period will be provided to students who experience a technical concern.

For any late submission of time-sensitive tasks, such as scheduled tests/exams, performance assessments/presentations, and/or scheduled practical assessments/labs, please apply for Special Consideration.

Detailed list of assessments where late submissions WILL be accepted but standard late penalties will apply: Minor Project, Complex Design Task, Student Engagement Tasks

Detailed list of assessments where late submissions WILL NOT be accepted unless Special

Consideration is granted: Quiz 1, 2 and 3.

Special Consideration

The Special Consideration Policy aims to support students who have been impacted by short-term circumstances or events that are serious, unavoidable and significantly disruptive, and which may affect their performance in assessment. If you experience circumstances or events that affect your ability to complete the assessments in this unit on time, please inform the convenor and submit a Special Consideration request through ask.mq.edu.au.

Assessment Tasks

Name	Weighting	Hurdle	Due
Quiz 1	10%	No	Week 4
Quiz 2	10%	Yes	Week 7
Minor Project	20%	No	Week 8
Quiz 3	10%	No	Week 11
Complex Design Task	40%	Yes	Week 13
Student Engagement	10%	No	All weeks

Quiz 1

Assessment Type [1]: Quiz/Test
Indicative Time on Task [2]: 3 hours
Due: **Week 4**
Weighting: **10%**

The first in a series of Quizzes that covers the material taught to date in the unit. This quiz will concentrate on Numbers, Boolean Algebra, Karnaugh Maps, Sum of Products and Combinatorial Logic.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

Quiz 2

Assessment Type [1]: Quiz/Test
Indicative Time on Task [2]: 3 hours
Due: **Week 7**
Weighting: **10%**
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

The second in a series of Quizzes that covers the material taught to date in the unit. This quiz will concentrate on Sequential logic, Counters and State Machines

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Design fast and efficient combinatorial logic circuits at the gate level.

Minor Project

Assessment Type [1]: Design Task
Indicative Time on Task [2]: 15 hours
Due: **Week 8**
Weighting: **20%**

This is the first design assignment. You will take the knowledge about digital circuits presented so far and design a circuit to perform a given task.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

Quiz 3

Assessment Type [1]: Quiz/Test

Indicative Time on Task [2]: 3 hours
Due: **Week 11**
Weighting: **10%**

The third in a series of Quizzes that covers the material taught to date in the unit. This quiz will concentrate on HDL

On successful completion you will be able to:

- Design fast and efficient combinatorial logic circuits at the gate level.
- Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA
- Describe the principle and operation of field programmable gate arrays (FPGAs)

Complex Design Task

Assessment Type [1]: Design Task
Indicative Time on Task [2]: 25 hours
Due: **Week 13**
Weighting: **40%**
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

This assignment is a design assignment. You must design and present a state machine to solve the project outline given. A rubric will be issued to indicate what is being looked for in the assignment.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Design fast and efficient combinatorial logic circuits at the gate level.
- Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA

Student Engagement

Assessment Type [1]: Programming Task

Indicative Time on Task [2]: 12 hours
Due: **All weeks**
Weighting: **10%**

Students are expected to actively participate in the programming learning activities with a developing level of independence. Before each practical session students may be required to complete preparatory work in a log book. During the practical sessions students must also complete their work and keep a log book of their work.

On successful completion you will be able to:

- Apply Karnaugh-map and boolean algebra techniques to minimise combinatorial logic truth tables.
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Design fast and efficient combinatorial logic circuits at the gate level.
- Implement digital logic circuits and systems using individual integrated circuit components, as well as with hardware description language on an FPGA

---

[1] If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- the Writing Centre for academic skills support.

[2] Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation

Delivery and Resources

Each week students are expected to attend a 2-hour lecture and a 3-hour practical session on campus. There is pre-work that needs to be completed before each practical session, which may include watching videos and completing exercises.

This is a hands-on unit, centred around physical circuits. We will be using physical trainer boards to build digital circuits and experiment with those circuits, along with buidling full digital systems on an FPGA. All students are expected to attend their practical session on campus to access the hardware. To describe and implement digital circuits and systems on an FPGA, we will be using Xilinx Vivado Design tools which allows simulation and synthesis of designs. The software is available on the computers in the lab, but students are also expected to install it onto their own computers so that they can do the pre-work and complex design task. You will need a Windows laptop with a minimum of 8 GB RAM and ~40 GB hard drive space.

The text book for this unit is *Introduction to Logic Circuits & Logic Design with Verilog*, 2nd Edition by Brock J. LaMeres. It is available free of charge to students through the library. You will find a link to the textbook through Leganto on the iLearn website.

Unit Schedule

Topics covered in this unit include: analog-to-digital conversion, Boolean algebra, logic gates, digital circuit design techniques, combinational logic, state machines, hardware description languages, and field programmable gate arrays.

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://policies.mq.edu.au). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy
- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Assessment Procedure
- Complaints Resolution Procedure for Students and Members of the Public
- Special Consideration Policy

Students seeking more policy resources can visit Student Policies (https://students.mq.edu.au/support/study/policies). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit Policy Central (https://policies.mq.edu.au) and use the search tool.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/admin/other-resources/student-conduct

Results

Results published on platform other than eStudent, (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Academic Integrity

At Macquarie, we believe academic integrity – honesty, respect, trust, responsibility, fairness and courage – is at the core of learning, teaching and research. We recognise that meeting the

expectations required to complete your assessments can be challenging. So, we offer you a range of resources and services to help you reach your potential, including free online writing and maths support, academic skills development and wellbeing consultations.

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

The Writing Centre

The Writing Centre provides resources to develop your English language proficiency, academic writing, and communication skills.

- Workshops
- Chat with a WriteWISE peer writing leader
- Access StudyWISE
- Upload an assignment to Studiosity
- Complete the Academic Integrity Module

The Library provides online and face to face support to help you find and use relevant information resources.

- Subject and Research Guides
- Ask a Librarian

Student Services and Support

Macquarie University offers a range of Student Support Services including:

- IT Support
- Accessibility and disability support with study
- Mental health support
- Safety support to respond to bullying, harassment, sexual harassment and sexual assault
- Social support including information about finances, tenancy and legal issues
- Student Advocacy provides independent advice on MQ policies, procedures, and processes

Student Enquiries

Got a question? Ask us via AskMQ, or contact Service Connect.

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Changes from Previous Offering

Student engagement is no longer a hurdle requirement.

Engineers Australia Competency Mapping

EA Competency Standard		Unit Learning Outcomes
Knowledge and Skill Base	1.1 Comprehensive, theory-based understanding of the underpinning fundamentals applicable to the engineering discipline.	2
	1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing.	1,3
	1.3 In-depth understanding of specialist bodies of knowledge	1,4,5
	1.4 Discernment of knowledge development and research directions	
	1.5 Knowledge of engineering design practice	
	1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice.	
Engineering Application Ability	2.1 Application of established engineering methods to complex problem solving	1,4,5
	2.2 Fluent application of engineering techniques, tools and resources.	1
	2.3 Application of systematic engineering synthesis and design processes.	4
	2.4 Application of systematic approaches to the conduct and management of engineering projects.	
Professional and Personal Attributes	3.1 Ethical conduct and professional accountability.	
	3.2 Effective oral and written communication in professional and lay domains.	
	3.3 Creative, innovative and pro-active demeanour.	
	3.4 Professional use and management of information.	
	3.5 Orderly management of self, and professional conduct.	
	3.6 Effective team membership and team leadership	