



ELEC4250

System on Chip Design

Session 2, In person-scheduled-weekday, North Ryde 2023

School of Engineering

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General Information

Unit convenor and teaching staff

Unit Convenor

Alan Kan

alan.kan@mq.edu.au

Contact via Private message on iLearn

Level 1, 50 Waterloo Road

Wed 9-10 am, Confirm location via Private message

Credit points

10

Prerequisites

ELEC3042 or ELEC342 or Admission to MEngElecEng

Corequisites

Co-badged status

Unit description

This unit aims to provide an understanding of the concepts, architectures, design tools and methods for developing System-on-Chip (SoC) solutions. The unit culminates in a project where students develop a SoC solution from high-level functional specifications through to design, implementation and testing on real hardware using industry standard hardware description and software programming languages and tools.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at <https://www.mq.edu.au/study/calendar-of-dates>

Learning Outcomes

On successful completion of this unit, you will be able to:

ULO1: Articulate a mature knowledge of what a System-on-Chip system is, and its constituent components.

ULO2: Investigate, document, and convey issues in hardware/software interface design.

ULO3: Work within the constraints imposed by the availability of resources on the System-on-Chip platform to produce designs that meet user requirements.

ULO4: Design and test System-on-Chip solutions on real hardware using standard

hardware description and software programming languages.

ULO5: Prepare design documents and reports and communicate and explain design decisions.

General Assessment Information

Grading and passing requirement for unit

There are three quizzes, one assignment and one design project for this unit. Quizzes will be conducted on iLearn. Assessment of the assignment is through a written report and code. Assessment of the project is through a written report, code, and oral defense. They will be due according to the given schedule.

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD) and pass the hurdle requirements.

For further details about grading, please refer below in the policies and procedures section.

Hurdle Requirements

The assignment is a hurdle. A grade of 50% or more in the assignment is required as a condition of passing this unit. If you do not pass the hurdle requirement on the first attempt, detailed feedback will be provided along with a second attempt. You must address the feedback provided sufficiently in your second attempt of the assignment. The second attempt at the hurdle assessment is graded as pass/fail. **The maximum grade for a second attempt is the hurdle threshold grade.**

Late submissions and Resubmissions

Resubmission of work is not allowed.

Unless a Special Consideration request has been submitted and approved, a 5% penalty (of the total possible mark of the task) will be applied for each day a written report or presentation assessment is not submitted, up until the 7th day (including weekends). After the 7th day, a grade of '0' will be awarded even if the assessment is submitted. The submission time for all uploaded assessments is 11:55 pm. A 1-hour grace period will be provided to students who experience a technical concern.

For any late submission of time-sensitive tasks, such as scheduled tests/exams, performance assessments/presentations, and/or scheduled practical assessments/labs, please apply for Special Consideration.

Detailed list of assessments where late submissions WILL be accepted but standard late penalties will apply: Assignment Report and Code, Project Report

Detailed list of assessments where late submissions WILL NOT be accepted unless Special Consideration is granted: Quizzes, Project Defense

Special Consideration

The Special Consideration Policy aims to support students who have been impacted by short-term circumstances or events that are serious, unavoidable and significantly disruptive, and

which may affect their performance in assessment. If you experience circumstances or events that affect your ability to complete the assessments in this unit on time, please inform the convenor and submit a Special Consideration request through ask.mq.edu.au.

Assessment Tasks

Name	Weighting	Hurdle	Due
Quizzes	30%	No	Week 4, 6, 10
Assignment	25%	Yes	Week 7
Project Implementation and Report	20%	No	Week 12
Project Defense	25%	No	Week 13

Quizzes

Assessment Type ¹: Quiz/Test

Indicative Time on Task ²: 15 hours

Due: **Week 4, 6, 10**

Weighting: **30%**

Quizzes during session

On successful completion you will be able to:

- Articulate a mature knowledge of what a System-on-Chip system is, and its constituent components.

Assignment

Assessment Type ¹: Report

Indicative Time on Task ²: 20 hours

Due: **Week 7**

Weighting: **25%**

This is a hurdle assessment task (see [assessment policy](#) for more information on hurdle assessment tasks)

Students will implement and report on their design of a hardware module

On successful completion you will be able to:

- Articulate a mature knowledge of what a System-on-Chip system is, and its constituent

components.

- Investigate, document, and convey issues in hardware/software interface design.
- Work within the constraints imposed by the availability of resources on the System-on-Chip platform to produce designs that meet user requirements.
- Design and test System-on-Chip solutions on real hardware using standard hardware description and software programming languages.
- Prepare design documents and reports and communicate and explain design decisions.

Project Implementation and Report

Assessment Type ¹: Design Task

Indicative Time on Task ²: 45 hours

Due: **Week 12**

Weighting: **20%**

Project Implementation and Report (2000-word equivalent)

On successful completion you will be able to:

- Investigate, document, and convey issues in hardware/software interface design.
- Work within the constraints imposed by the availability of resources on the System-on-Chip platform to produce designs that meet user requirements.
- Prepare design documents and reports and communicate and explain design decisions.

Project Defense

Assessment Type ¹: Viva/oral examination

Indicative Time on Task ²: 5 hours

Due: **Week 13**

Weighting: **25%**

Project Defense

On successful completion you will be able to:

- Articulate a mature knowledge of what a System-on-Chip system is, and its constituent components.
- Investigate, document, and convey issues in hardware/software interface design.
- Work within the constraints imposed by the availability of resources on the System-on-

Chip platform to produce designs that meet user requirements.

- Design and test System-on-Chip solutions on real hardware using standard hardware description and software programming languages.
- Prepare design documents and reports and communicate and explain design decisions.

¹ If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- the [Writing Centre](#) for academic skills support.

² Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation

Delivery and Resources

This unit consists of a 2-hour lecture and 3-hour practical session each week on campus. Students are expected to attend both, and complete the necessary pre-work prior to attending the lecture.

You will be using the Xilinx Vivado HL Design Edition to program a Zynq Ultrascale+ MPSoC (on an Ultra96 development board) for your practicals and assessments. The Vivado design tools will be available on the computers in the lab but you should also install it onto your own laptop so that you can work on the assignment and project at home. You will need access to a Windows laptop with at least 8 GB RAM and ~41 GB of free hard drive space.

Access to the Ultra96 development board will only be available during the weekly practical. Hence, it is important to attend all practicals to ensure you have sufficient time to complete the practicals and assessments. While some practical weeks are dedicated to working on the project, students must also spend sufficient time outside of class in order to complete the project.

There is no textbook for this unit. Additional reading and learning resources will be provided through the unit's iLearn page.

Unit Schedule

This unit covers high level synthesis, hardware/software partitioning, Zynq Ultrascale+ MPSoC Architecture, and PYNQ. The unit uses both C and Python languages. Hence, students are expected to be able to write a computer program prior to attempting this unit. They should also have a basic understanding of computing architecture.

Policies and Procedures

Macquarie University policies and procedures are accessible from [Policy Central \(https://policies.mq.edu.au\)](https://policies.mq.edu.au). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- [Academic Appeals Policy](#)
- [Academic Integrity Policy](#)
- [Academic Progression Policy](#)
- [Assessment Policy](#)
- [Fitness to Practice Procedure](#)
- [Assessment Procedure](#)
- [Complaints Resolution Procedure for Students and Members of the Public](#)
- [Special Consideration Policy](#)

Students seeking more policy resources can visit [Student Policies](https://students.mq.edu.au/support/study/policies) (<https://students.mq.edu.au/support/study/policies>). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit [Policy Central](https://policies.mq.edu.au) (<https://policies.mq.edu.au>) and use the [search tool](#).

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: <https://students.mq.edu.au/admin/other-resources/student-conduct>

Results

Results published on platform other than [eStudent](#), (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in [eStudent](#). For more information visit ask.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Academic Integrity

At Macquarie, we believe [academic integrity](#) – honesty, respect, trust, responsibility, fairness and courage – is at the core of learning, teaching and research. We recognise that meeting the expectations required to complete your assessments can be challenging. So, we offer you a range of resources and services to help you reach your potential, including free [online writing and maths support](#), [academic skills development](#) and [wellbeing consultations](#).

Student Support

Macquarie University provides a range of support services for students. For details, visit <http://students.mq.edu.au/support/>

The Writing Centre

[The Writing Centre](#) provides resources to develop your English language proficiency, academic writing, and communication skills.

- [Workshops](#)
- [Chat with a WriteWISE peer writing leader](#)

- [Access StudyWISE](#)
- [Upload an assignment to Studiosity](#)
- [Complete the Academic Integrity Module](#)

The Library provides online and face to face support to help you find and use relevant information resources.

- [Subject and Research Guides](#)
- [Ask a Librarian](#)

Student Services and Support

Macquarie University offers a range of [Student Support Services](#) including:

- [IT Support](#)
- [Accessibility and disability support](#) with study
- Mental health [support](#)
- [Safety support](#) to respond to bullying, harassment, sexual harassment and sexual assault
- [Social support](#) including information about finances, tenancy and legal issues
- [Student Advocacy](#) provides independent advice on MQ policies, procedures, and processes

Student Enquiries

Got a question? Ask us via [AskMQ](#), or contact [Service Connect](#).

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the [Acceptable Use of IT Resources Policy](#). The policy applies to all who connect to the MQ network including students.

Changes from Previous Offering

The assignment has been changed to a hurdle assessment to ensure a student has attained a minimum level of competency for the unit before the last day to withdraw without academic penalty.

Engineers Australia Competency Mapping

EA Competency Standard	Unit Learning Outcomes

Knowledge and Skill Base	1.1 Comprehensive, theory-based understanding of the underpinning fundamentals applicable to the engineering discipline.	
	1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing.	1
	1.3 In-depth understanding of specialist bodies of knowledge	1,2
	1.4 Discernment of knowledge development and research directions	
	1.5 Knowledge of engineering design practice	2,3,4
	1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice.	2,3
Engineering Application Ability	2.1 Application of established engineering methods to complex problem solving	3,4
	2.2 Fluent application of engineering techniques, tools and resources.	3,4
	2.3 Application of systematic engineering synthesis and design processes.	3,4
	2.4 Application of systematic approaches to the conduct and management of engineering projects.	
Professional and Personal Attributes	3.1 Ethical conduct and professional accountability.	
	3.2 Effective oral and written communication in professional and lay domains.	2,5
	3.3 Creative, innovative and pro-active demeanour.	
	3.4 Professional use and management of information.	
	3.5 Orderly management of self, and professional conduct.	
	3.6 Effective team membership and team leadership	