ELEC2042

Digital Circuits and Systems

Session 2, In person-scheduled-weekday, North Ryde 2024

School of Engineering

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General Information

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Credit points
10

Prerequisites
COMP115 or COMP1000

Corequisites

Co-badged status

Unit description
This unit aims to provide students with an understanding of, and fluency in, combinational and sequential logic design techniques commonly used in the design of large-scale digital systems. Students will apply this knowledge to the design and implementation of digital circuits and systems.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

ULO1: Demonstrate an understanding of different number systems used in digital systems and be able to convert between them

ULO2: Design fast and efficient logic circuits by applying standard minimisation techniques

ULO3: Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

ULO4: Describe and document digital logic circuits and systems using industry-standard languages and tools

ULO5: Implement digital logic circuits and systems in hardware

General Assessment Information

Grading and passing requirement for unit

There are three quizzes, one minor project and one complex design task for this unit. Quizzes will be conducted in-class. Assessment of the minor project is through a written report and circuit model in software. Assessment of the complex design task is through a written report and circuit model in software.

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD) and pass the hurdle requirements.

For further details about grading, please refer below in the policies and procedures section.

Hurdle Requirements

Quiz 2 and Quiz 3 have a hurdle requirement. Achieving a grade of 40% or more is required in these tasks as a condition of passing this unit. If you do not pass the hurdle requirement for Quiz 2, you may be given a second attempt if you demonstrated that you made a reasonable first attempt. Similarly, if you do not pass the hurdle requirement for Quiz 3 on the first attempt, you may be given a second attempt if you demonstrated that you made a reasonable first attempt.

All second attempts at the hurdle assessment will be graded as pass/fail. **The maximum grade for a second attempt is the hurdle threshold grade**.

Late submissions and Resubmissions

Resubmission of work is not allowed.

Unless a Special Consideration request has been submitted and approved, a 5% penalty (of the total possible mark of the task) will be applied for each day a written report or presentation assessment is not submitted, up until the 7th day (including weekends). After the 7th day, a grade of '0' will be awarded even if the assessment is submitted. The submission time for all uploaded assessments is 11:59 pm. A 1-hour grace period will be provided to students who experience a technical concern.

For any late submission of time-sensitive tasks, such as scheduled tests/exams, performance assessments/presentations, and/or scheduled practical assessments/labs, please apply for Special Consideration.

Detailed list of assessments where late submissions WILL be accepted but standard late penalties will apply: Minor Project, Complex Design Task, Student Engagement Tasks.

Detailed list of assessments where late submissions WILL NOT be accepted unless Special Consideration is granted: Quiz 1, 2 and 3.

Special Consideration

The Special Consideration Policy aims to support students who have been impacted by short-term circumstances or events that are serious, unavoidable and significantly disruptive, and which may affect their performance in assessment. If you experience circumstances or events that affect your ability to complete the assessments in this unit on time, please inform the convenor and submit a Special Consideration request through ask.mq.edu.au.

Assessment Tasks

Name	Weighting	Hurdle	Due	Groupwork/Individual	Short Extension	AI Approach
Complex Design Task	30%	No	Week 13		No	
Minor Project	20%	No	Week 7		No	
Quiz 1	5%	No	Week 4		No	
Quiz 2	10%	Yes	Week 8		No	
Quiz 3	15%	Yes	Week 12		No	
Student Engagement	20%	No	All Session		No	

Complex Design Task

Assessment Type [1]: Design Task

Indicative Time on Task [2]: 25 hours
Due: **Week 13**
Weighting: **30%**
Groupwork/Individual:
Short extension [3]: No
AI Approach:

This assignment is a design assignment. You must design and present a state machine to solve the project outline given. A rubric will be issued to indicate what is being looked for in the assignment.

On successful completion you will be able to:

- Demonstrate an understanding of different number systems used in digital systems and be able to convert between them
- Design fast and efficient logic circuits by applying standard minimisation techniques
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Describe and document digital logic circuits and systems using industry-standard languages and tools
- Implement digital logic circuits and systems in hardware

Minor Project

Assessment Type [1]: Design Task
Indicative Time on Task [2]: 15 hours
Due: **Week 7**
Weighting: **20%**
Groupwork/Individual:
Short extension [3]: No
AI Approach:

This is the first design assignment. You will take the knowledge about digital circuits presented so far and design a circuit to perform a given task.

On successful completion you will be able to:

- Design fast and efficient logic circuits by applying standard minimisation techniques
- Relate state-diagrams, truth tables, wave forms and logic equations as different

representations of the same synchronous sequential machine.
- Describe and document digital logic circuits and systems using industry-standard languages and tools

Quiz 1

Assessment Type [1]: Quiz/Test
Indicative Time on Task [2]: 3 hours
Due: **Week 4**
Weighting: **5%**
Groupwork/Individual:
Short extension [3]: No
AI Approach:

The first in a series of Quizzes that covers the material taught to date in the unit.

On successful completion you will be able to:
- Demonstrate an understanding of different number systems used in digital systems and be able to convert between them
- Design fast and efficient logic circuits by applying standard minimisation techniques
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.

Quiz 2

Assessment Type [1]: Quiz/Test
Indicative Time on Task [2]: 3 hours
Due: **Week 8**
Weighting: **10%**
Groupwork/Individual:
Short extension [3]: No
AI Approach:
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

The second in a series of Quizzes that covers the material taught to date in the unit.

On successful completion you will be able to:

- Design fast and efficient logic circuits by applying standard minimisation techniques
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Describe and document digital logic circuits and systems using industry-standard languages and tools

Quiz 3

Assessment Type [1]: Quiz/Test
Indicative Time on Task [2]: 3 hours
Due: **Week 12**
Weighting: **15%**
Groupwork/Individual:
Short extension [3]: No
AI Approach:
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

The third in a series of Quizzes covers all material taught in the unit

On successful completion you will be able to:

- Demonstrate an understanding of different number systems used in digital systems and be able to convert between them
- Design fast and efficient logic circuits by applying standard minimisation techniques
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Describe and document digital logic circuits and systems using industry-standard languages and tools

Student Engagement

Assessment Type [1]: Problem set
Indicative Time on Task [2]: 12 hours
Due: **All Session**
Weighting: **20%**
Groupwork/Individual:
Short extension [3]: No
AI Approach:

Students are expected to actively participate in learning activities with a developing level of independence. Before each practical session students may be required to complete preparatory work in a log book. During the practical sessions students must also complete their work and keep a log book of their work.

On successful completion you will be able to:

- Demonstrate an understanding of different number systems used in digital systems and be able to convert between them
- Design fast and efficient logic circuits by applying standard minimisation techniques
- Relate state-diagrams, truth tables, wave forms and logic equations as different representations of the same synchronous sequential machine.
- Describe and document digital logic circuits and systems using industry-standard languages and tools
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[1] If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- Academic Success for academic skills support.

[2] Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation.

[3] An automatic short extension is available for some assessments. Apply through the Service Connect Portal.

Delivery and Resources

Each week students are expected to attend a 2-hour lecture and a 3-hour practical session on campus. The students will be provided with lecture slides each week in iLearn. Practical sheets and projects will also be posted to iLearn. There may be pre-work that needs to be completed before each practical session, which may include watching videos and completing exercises.

This is a hands-on unit, centred around digital logic circuits. We will be using physical trainer boards to build digital circuits and experiment with those circuits, along with building full digital systems using simulation software tools. All students are expected to attend their practical session on campus to access the hardware.

The following textbooks will be used:

- *Digital Design and Computer Architecture (MIPS Version),* 2nd Edition by D. M. Harris

and S. L. Harris

- *Digital Design with an Introduction to the Verilog HDL, VHDL and System Verilog*, 6th Edition by M. M. R. Mano and M. D. Ciletti

Both books are available free of charge to students through the library.

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://policies.mq.edu.au). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy
- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Assessment Procedure
- Complaints Resolution Procedure for Students and Members of the Public
- Special Consideration Policy

Students seeking more policy resources can visit Student Policies (https://students.mq.edu.au/support/study/policies). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit Policy Central (https://policies.mq.edu.au) and use the search tool.

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/admin/other-resources/student-conduct

Results

Results published on platform other than eStudent, (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit connect.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Academic Integrity

At Macquarie, we believe academic integrity – honesty, respect, trust, responsibility, fairness and courage – is at the core of learning, teaching and research. We recognise that meeting the expectations required to complete your assessments can be challenging. So, we offer you a range of resources and services to help you reach your potential, including free online writing and maths support, academic skills development and wellbeing consultations.

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

The Writing Centre

The Writing Centre provides resources to develop your English language proficiency, academic writing, and communication skills.

- Workshops
- Chat with a WriteWISE peer writing leader
- Access StudyWISE
- Upload an assignment to Studiosity
- Complete the Academic Integrity Module

The Library provides online and face to face support to help you find and use relevant information resources.

- Subject and Research Guides
- Ask a Librarian

Student Services and Support

Macquarie University offers a range of Student Support Services including:

- IT Support
- Accessibility and disability support with study
- Mental health support
- Safety support to respond to bullying, harassment, sexual harassment and sexual assault
- Social support including information about finances, tenancy and legal issues
- Student Advocacy provides independent advice on MQ policies, procedures, and processes

Student Enquiries

Got a question? Ask us via the Service Connect Portal, or contact Service Connect.

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Engineers Australia Competency Mapping

EA Competency Standard		Unit Learning Outcomes
Knowledge and Skill Base	1.1 Comprehensive, theory-based understanding of the underpinning fundamentals applicable to the engineering discipline.	ULO2
	1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing.	ULO1, ULO3
	1.3 In-depth understanding of specialist bodies of knowledge	ULO1, ULO4, ULO5
	1.4 Discernment of knowledge development and research directions	
	1.5 Knowledge of engineering design practice	ULO2, ULO5
	1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice.	
Engineering Application Ability	2.1 Application of established engineering methods to complex problem solving	ULO1, ULO3, ULO4, ULO5
	2.2 Fluent application of engineering techniques, tools and resources.	ULO1, ULO2
	2.3 Application of systematic engineering synthesis and design processes.	ULO4
	2.4 Application of systematic approaches to the conduct and management of engineering projects.	
Professional and Personal Attributes	3.1 Ethical conduct and professional accountability.	
	3.2 Effective oral and written communication in professional and lay domains.	
	3.3 Creative, innovative and pro-active demeanour.	
	3.4 Professional use and management of information.	
	3.5 Orderly management of self, and professional conduct.	
	3.6 Effective team membership and team leadership	

Changes since First Published

Date	Description
02/08/2024	Tutor information is updated.

Unit information based on version 2024.02 of the Handbook