



ELEC4250

System on Chip Design

Session 2, In person-scheduled-weekday, North Ryde 2026

School of Engineering

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General Information

Unit convenor and teaching staff

Convenor

Yiqing Lu

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9WW 2111

Fridays 3-5 pm

Credit points

10

Prerequisites

ELEC3042 or Admission to MEngElecEng

Corequisites

Co-badged status

Unit description

This unit aims to provide an understanding of the concepts, architectures, design tools and methods for developing System-on-Chip (SoC) solutions. The unit culminates in a project where students develop a SoC solution from high-level functional specifications through to design, implementation and testing on real hardware using industry standard hardware description and software programming languages and tools.

Learning in this unit enhances student understanding of global challenges identified by the United Nations Sustainable Development Goals ([UNSDGs](#)) Quality Education; Affordable and Clean Energy; Industry, Innovation and Infrastructure

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at <https://www.mq.edu.au/study/calendar-of-dates>

Learning Outcomes

On successful completion of this unit, you will be able to:

ULO1: Articulate a mature knowledge of what a System-on-Chip system is, and its constituent components.

ULO2: Investigate, document, and convey issues in hardware/software interface design.

ULO3: Work within the constraints imposed by the availability of resources on the

System-on-Chip platform to produce designs that meet user requirements.

ULO4: Design and test System-on-Chip solutions on real hardware using standard hardware description and software programming languages.

ULO5: Prepare design documents and reports and communicate and explain design decisions.

General Assessment Information

Grading and passing requirement for unit

In order to pass this unit, a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD). For further details about grading, please refer below in the policies and procedures section.

Release dates

Assignment: To be released no later than 17 Aug.

Lab Portfolio tasks: To be released weekly from Week 2 to Week 8.

Project: To be released no later than 6 Oct.

Late submissions and Resubmissions

Resubmission of work is allowed before the due date.

Unless a Special Consideration request has been submitted and approved, a 5% penalty (of the total possible mark of the task) will be applied for each day an assessment is not submitted, up until the 7th day (including weekends). After the 7th day, a grade of '0' will be awarded even if the assessment is submitted. The submission time for all uploaded assessments is **11:55 pm**. A 1-hour grace period will be provided to students who experience a technical concern.

For any late submission of time-sensitive tasks, such as scheduled oral defences, performance assessments/presentations, and/or scheduled practical assessments/labs, students need to submit an application for [Special Consideration](#).

Assessments where Late Submissions will be accepted

In this unit, late submissions will accepted as follows:

Assignment, Project – YES, Standard Late Penalty applies;

Lab Portfolio – NO, unless Special Consideration is Granted.

Short extensions

Students are allowed to request an extra 3 calendar days to complete Assignment. Short extensions do not apply to Lab Portfolio or Project.

Assessment Tasks

Name	Weighting	Hurdle	Due	Groupwork/Individual	Short Extension	AI Approach
<u>Assignment</u>	25%	No	13/09/2026	Individual	Yes	Open
<u>Lab Portfolio</u>	25%	No	04/10/2026	Individual	No	Open
<u>Major Project</u>	50%	No	04/11/2026	Individual and Group	No	Open

Assignment

Assessment Type ¹: Practice-based task

Indicative Time on Task ²: 25 hours

Due: **13/09/2026**

Weighting: **25%**

Groupwork/Individual: Individual

Short extension ³: Yes

AI Approach: Open

You will design, implement, validate, and report a SoC solution to a common type of computational task, within the constraints imposed by the available resources on the SoC platform.

On successful completion you will be able to:

- Work within the constraints imposed by the availability of resources on the System-on-Chip platform to produce designs that meet user requirements.
- Design and test System-on-Chip solutions on real hardware using standard hardware description and software programming languages.
- Prepare design documents and reports and communicate and explain design decisions.

Lab Portfolio

Assessment Type ¹: Portfolio

Indicative Time on Task ²: 10 hours

Due: **04/10/2026**

Weighting: **25%**

Groupwork/Individual: Individual

Short extension ³: No

AI Approach: Open

You will complete a series of practical tasks to consolidate knowledge and skills in design, implementation and testing of SoC solutions, supported by guided exercises provided in each session. You will submit a workshop report that demonstrates your laboratory work through the semester for assessment at the end of the session.

On successful completion you will be able to:

- Articulate a mature knowledge of what a System-on-Chip system is, and its constituent components.
- Investigate, document, and convey issues in hardware/software interface design.
- Design and test System-on-Chip solutions on real hardware using standard hardware description and software programming languages.

Major Project

Assessment Type ¹: Problem-based task

Indicative Time on Task ²: 50 hours

Due: **04/11/2026**

Weighting: **50%**

Groupwork/Individual: Individual and Group

Short extension ³: No

AI Approach: Open

You will conduct a project to design, implement, and test SoC solutions on real hardware to produce a SoC system that meet specific user requirements, and communicate the results in both written report and oral defense. Groups will present on the project and individual group members will also be expected to demonstrate their individual contribution.

On successful completion you will be able to:

- Articulate a mature knowledge of what a System-on-Chip system is, and its constituent components.
- Investigate, document, and convey issues in hardware/software interface design.
- Work within the constraints imposed by the availability of resources on the System-on-Chip platform to produce designs that meet user requirements.
- Design and test System-on-Chip solutions on real hardware using standard hardware description and software programming languages.
- Prepare design documents and reports and communicate and explain design decisions.

¹ If you need help with your assignment, please contact:

- the academic teaching staff in your unit for guidance in understanding or completing this type of assessment
- [Academic Success](#) for academic skills support.

² Indicative time-on-task is an estimate of the time required for completion of the assessment task and is subject to individual variation.

³ An automatic short extension is available for some assessments. Apply through the [Service Connect Portal](#).

Delivery and Resources

This unit consists of lectures (lectorials) and practical sessions on campus. Students are expected to attend both, **starting from Week 1**, and complete the necessary preparation prior to attending the classes.

The unit uses the Xilinx/AMD Vivado HL Design Edition and PYNQ to design SoC solutions on a PYNQ-Z2 development board for your practicals and assessments. The Vivado design tools will be available on the computers in the lab but you should also install it onto your own laptop so that you can work on the assignment and project at home. You will need access to a Windows laptop with at least 8 GB RAM and ~41 GB of free hard drive space. You will be able to borrow a PYNQ-Z2 development board from the School during the semester to ensure you have sufficient time to practice and complete the assessments. While some practical weeks are dedicated to working on the project, students must also spend sufficient time outside of class in order to complete the project.

Students are expected to be able to write a computer program prior to attempting this unit. They should also have a basic understanding of computer architecture. There is no textbook for this unit. Additional reading and learning resources will be provided through the unit's iLearn page.

Methods of communication

We will communicate with you via your university email and through announcements on iLearn. Queries can either be placed in the iLearn discussion forum, or sent to the unit convenor via the contact email with the unit code included in the subject.

Unit Schedule

Refer to iLearn for details.

Policies and Procedures

Macquarie University policies and procedures are accessible from [Policy Central](#) (<https://policies.mq.edu.au>). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- [Academic Appeals Policy](#)
- [Academic Integrity Policy](#)
- [Academic Progression Policy](#)
- [Assessment Policy](#)
- [Fitness to Practice Procedure](#)
- [Assessment Procedure](#)
- [Complaints Resolution Procedure for Students and Members of the Public](#)
- [Special Consideration Policy](#)

Students seeking more policy resources can visit [Student Policies](https://students.mq.edu.au/support/study/policies) (<https://students.mq.edu.au/support/study/policies>). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

To find other policies relating to Teaching and Learning, visit [Policy Central](https://policies.mq.edu.au) (<https://policies.mq.edu.au>) and use the [search tool](#).

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: <https://students.mq.edu.au/admin/other-resources/student-conduct>

Results

Results published on platform other than [eStudent](#), (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in [eStudent](#). For more information visit connect.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Academic Integrity

At Macquarie, we believe [academic integrity](#) – honesty, respect, trust, responsibility, fairness and courage – is at the core of learning, teaching and research. We recognise that meeting the expectations required to complete your assessments can be challenging. So, we offer you a range of resources and services to help you reach your potential, including free [online writing and maths support](#), [academic skills development](#) and [wellbeing consultations](#).

Student Support

Macquarie University provides a range of support services for students. For details, visit <http://students.mq.edu.au/support/>

Academic Success

[Academic Success](#) provides resources to develop your English language proficiency, academic writing, and communication skills.

- [Ask a Study Coach](#)
- [Access StudyWISE](#)
- [Upload an assignment to Studiosity](#)
- [Complete the Academic Integrity Module](#)

The Library provides online and face to face support to help you find and use relevant information resources.

- [Subject and Research Guides](#)
- [Ask a Librarian](#)

Student Services and Support

Macquarie University offers a range of [Student Support Services](#) including:

- [IT Support](#)
- [Accessibility and disability support](#) with study
- Mental health [support](#)
- [Safety support](#) to respond to bullying, harassment, sexual harassment and sexual assault
- [Social support including information about finances, tenancy and legal issues](#)
- [Student Advocacy](#) provides independent advice on MQ policies, procedures, and processes

Student Enquiries

Got a question? Ask us via the [Service Connect Portal](#), or contact [Service Connect](#).

IT Help

For help with University computer systems and technology, visit <https://students.mq.edu.au/support/technology/service-desk>.

When using the University's IT, you must adhere to the [Acceptable Use of IT Resources Policy](#). The policy applies to all who connect to the MQ network including students.

Changes from Previous Offering

Contents of the unit has been rearranged to deliver a coherent learning experience in alignment with the learning outcomes.

Engineers Australia Competency Mapping

EA Competency Standard		Unit Learning Outcomes
Knowledge and Skill Base	1.1 Comprehensive, theory-based understanding of the underpinning fundamentals applicable to the engineering discipline.	
	1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing.	ULO1
	1.3 In-depth understanding of specialist bodies of knowledge	ULO1, ULO2
	1.4 Discernment of knowledge development and research directions	
	1.5 Knowledge of engineering design practice	ULO2, ULO3, ULO4

	1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice.	ULO2, ULO3
Engineering Application Ability	2.1 Application of established engineering methods to complex problem solving	ULO3, ULO4
	2.2 Fluent application of engineering techniques, tools and resources.	ULO3, ULO4
	2.3 Application of systematic engineering synthesis and design processes.	ULO3, ULO4
	2.4 Application of systematic approaches to the conduct and management of engineering projects.	
Professional and Personal Attributes	3.1 Ethical conduct and professional accountability.	
	3.2 Effective oral and written communication in professional and lay domains.	ULO2, ULO5
	3.3 Creative, innovative and pro-active demeanour.	
	3.4 Professional use and management of information.	
	3.5 Orderly management of self, and professional conduct.	
	3.6 Effective team membership and team leadership	

Unit information based on version 2026.03 of the [Handbook](#)