# ELEC643

## Digital Systems Design

S2 Day 2018

*Dept of Engineering*

## Contents

# General Information

Unit convenor and teaching staff
lecturer
Yinan Kong
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E6B129
1pm to 2pm Tuesday

tutor
Naila Mukhtar
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E6B
3pm to 4pm Wednesday

Credit points
4

Prerequisites
Admission to MEng

Corequisites

Co-badged status

Unit description
This unit is a sequence of lectures and practical work on digital systems designs, including: behavioural specification and description; architecture and structure design; software/ hardware co-design; technology mapping, verification and test. For greater complexity we choose Field-Programmable Gate Arrays (FPGAs) and a variety of software provided by the manufacturer (Xilinx), including Boolean equations, schematic entry, state machines, and a high-level design language (VHDL), itself supporting a variety of modes. This unit gives students the skills and knowledge needed to design modern digital systems.

## Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

# Learning Outcomes

On successful completion of this unit, you will be able to:

Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.

Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.

Ability to conduct complex digital systems design within an integrated engineering team.

In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

# General Assessment Information

### Student Responsibilities

Be familiar with University policy and College procedures and act in accordance with those policy and procedures.

It is the responsibility of the student to retain a copy of any work submitted. Students must produce these documents upon request. Copies should be retained until the end of the grade appeal period each term.

Student is to perform the required due diligent for their assessment grade and rectify as soon as possible upon finding any errors.

### Practical sessions

There are twelve practical sessions (each of three hours duration) starting in Week 2. Students will work individually in the first four sessions and work in teams of two in the other eight. Students will attend one practical session each week. On the completion of each session, each individual or group must complete and submit a “check-list” that itemizes each section of the practical. Each item is to be initialed by the group members on completion of the work. Individual contribution and performance are assessed in group practicals.  Individual performance as recorded in copies of the practical notes and summarized by the check-list will be used in the assessment of individual practical work.

Food and drink are not permitted in the laboratory. Students will not be permitted to enter the laboratory without appropriate footwear. Thongs and sandals are not acceptable.

### Report and Assignment Tasks

Two reports are required. One is based on the first four practicals and the other is based on the two team projects. Each team is only required to submit one report. **Reports should be submitted by the next Monday following the completion of the last practical session covered by the report.**

### Assignment submissions and plagiarism policies

All assignments and reports must be submitted electronically through iLearn (in pdf format).

Submissions will undergo plagiarism checkers using the turnitin software and any work deemed to have 30% or higher similarity score may incur academic penalty. For more details on the policies of academic penalties relating to academic honesty, please refer to the policies and procedures section below.

Submissions are expected to be typed set in a logical layout and sequence. Markers WILL NOT grade poorly organized or illegible scans or drafts. The expected workload includes preparation of final copies and clear diagrams.

### Late submissions and Resubmissions

Late submissions will attract a penalty of 10% marks per day. Extenuating circumstances will be considered upon lodgment of an application for special consideration.

Resubmissions of work are not allowed.

### Grading and passing requirement for unit

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD).

For further details about grading, please refer below in the policies and procedures section.

### Hurdle Requirement

The final examination is a hurdle requirement because it is the only reliable assessment of individual performance for this unit. A passing grade of 50% or more in the final examination is a condition of passing this unit.

## Assessment Tasks

| Name | Weighting | Hurdle | Due |
|---|---|---|---|
| Practical 1 | 2% | No | Week 2 |
| Practical 2 | 2% | No | Week 3 |
| Practical 3 | 3% | No | Week 4 |
| Practical 4 | 3% | No | Week 5 |
| Report 1 | 3% | No | Week 6 |
| Practical 5 | 2% | No | Week 6 |
| Practical 6 | 2% | No | Week 7 |

| Name | Weighting | Hurdle | Due |
|---|---|---|---|
| Practical 7 | 2% | No | Week 8 |
| Practical 8 | 2% | No | Week 9 |
| Project 1 Deliverables | 4% | No | Week 9 |
| Practical 9 | 2% | No | Week 10 |
| Practical 10 | 2% | No | Week 11 |
| Practical 11 | 2% | No | Week 12 |
| Practical 12 | 2% | No | Week 13 |
| Project 2 Deliverables | 4% | No | Week 13 |
| Report 2 | 3% | No | Week 14 |
| Exam | 60% | Yes | Exam Period |

## Practical 1

Due: **Week 2**
Weighting: **2%**

**Schematic Capture and Hierarchical Design**

On successful completion you will be able to:

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.

## Practical 2

Due: **Week 3**
Weighting: **2%**

**Getting Started with VHDL and Modelsim**

On successful completion you will be able to:

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.

## Practical 3

Due: **Week 4**
Weighting: **3%**

**Basic VHDL Design Examples**

On successful completion you will be able to:

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.

## Practical 4

Due: **Week 5**
Weighting: **3%**

**Basic VHDL Design Examples**

On successful completion you will be able to:

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.

## Report 1

Due: **Week 6**
Weighting: **3%**

Report on Practical 1 to 4

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.

## Practical 5

Due: **Week 6**
Weighting: **2%**

**Team Project – Computer Design**

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

## Practical 6

Due: **Week 7**
Weighting: **2%**

**Team Project – Computer Design**

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

## Practical 7

Due: **Week 8**
Weighting: **2%**

**Team Project – Computer Design**

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

## Practical 8

Due: **Week 9**
Weighting: **2%**

**Team Project – Computer Design**

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

## Project 1 Deliverables

Due: **Week 9**
Weighting: **4%**

Project 1 Deliverables

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

## Practical 9

Due: **Week 10**
Weighting: **2%**

**Team Project – Traffic Light Controller Design and Implementation**

On successful completion you will be able to:

- Ability to conduct complex digital systems design within an integrated engineering team.

## Practical 10

Due: **Week 11**
Weighting: **2%**

**Team Project – Traffic Light Controller Design and Implementation**

On successful completion you will be able to:

- Ability to conduct complex digital systems design within an integrated engineering team.

## Practical 11

Due: **Week 12**
Weighting: **2%**

**Team Project – Traffic Light Controller Design and Implementation**

On successful completion you will be able to:

- Ability to conduct complex digital systems design within an integrated engineering team.

## Practical 12

Due: **Week 13**
Weighting: **2%**

**Team Project – Traffic Light Controller Design and Implementation**

On successful completion you will be able to:

- Ability to conduct complex digital systems design within an integrated engineering team.

## Project 2 Deliverables

Due: **Week 13**
Weighting: **4%**

Project 2 Deliverables

On successful completion you will be able to:

- Ability to conduct complex digital systems design within an integrated engineering team.

## Report 2

Due: **Week 14**
Weighting: **3%**

Report 2 on Project 1 and 2

On successful completion you will be able to:

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- Ability to conduct complex digital systems design within an integrated engineering team.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

## Exam

Due: **Exam Period**
Weighting: **60%**
**This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)**

Exam (one 3-hour closed-book exam)

On successful completion you will be able to:

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.
- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- Ability to conduct complex digital systems design within an integrated engineering team.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

# Delivery and Resources

| | |
|---|---|
| Lectures | There is one lecture ahead of the practical session each week. Lecture and practical topics are provided in the (attached) timetable. Lecture slides and practical notes are all accessible on iLearn from the beginning of the unit delivery. It is strongly recommended that students preview the corresponding lecture slides and practical notes to ensure their efficient work at each practical session.<br><br>From time to time, important announcements and notices will be made in the lectures. It is the responsibility of the student to be aware of these announcements and notices. |
| Technology used and required | Technology used: Xilinx FPGAs, Xilinx ISE & XST and VHDL<br><br>Technology required: microcontrollers, programmable logic devices, e.g. GAL, PAL, etc. |

| | |
|---|---|
| Extension requests | Must be supported by evidence of medical conditions or misadventure. |
| Text book | Charles, R. H. and John, L. K., “Digital Systems Design Using VHDL”, Second edition, Thompson, 2008 |

| | |
|---|---|
| Reference book(s) | Vahid, F. and Lysecky, R., VHDL For Digital Design, Wiley 2007<br>Weste, N. and Harris, D., “CMOS VLSI Design -- A Circuit and Systems Perspecitive”, 3rd ed., (Addison-Wesley 2004)<br>Andrew Rushton, “VHDL for Logic Synthesis (Second Edition)”, John Wiley and Sons, 2001 |
| Notes | Notes for the practical sessions are available online. Each student is required to preview the corresponding notes before each practical session. |

# Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy

- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Grade Appeal Policy
- Complaint Management Procedure for Students and Members of the Public
- Special Consideration Policy *(**Note:** The Special Consideration Policy is effective from 4 December 2017 and replaces the Disruption to Studies Policy.)*

Undergraduate students seeking more policy resources can visit the Student Policy Gateway (https://students.mq.edu.au/support/study/student-policy-gateway). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

If you would like to see all the policies relevant to Learning and Teaching visit Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central).

## Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/study/getting-started/student-conduct

## Results

Results shown in *iLearn*, or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au.

# Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

## Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

# Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

## Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

## IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

# Graduate Capabilities

## Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

### Learning outcomes

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- Ability to conduct complex digital systems design within an integrated engineering team.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Report 1
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables
- Practical 9
- Practical 10
- Practical 11
- Practical 12
- Project 2 Deliverables
- Report 2
- Exam

## Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

### Learning outcome

- Ability to conduct complex digital systems design within an integrated engineering team.

### Assessment tasks

- Practical 9
- Practical 10
- Practical 11
- Practical 12
- Project 2 Deliverables
- Report 2
- Exam

## Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

### Learning outcomes

- Ability to conduct complex digital systems design within an integrated engineering team.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables

- Practical 9
- Practical 10
- Practical 11
- Practical 12
- Project 2 Deliverables
- Report 2
- Exam

## Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

### Learning outcomes

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables
- Report 2
- Exam

## Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to

critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

### Learning outcomes

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Practical 1
- Practical 2
- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables
- Report 2
- Exam

## Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

### Learning outcomes

- Conceptual understanding of the FPGA and VHDL concepts which underpin the subject.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Practical 1
- Practical 2

- Practical 3
- Practical 4
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables
- Report 2
- Exam

## Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

### Learning outcomes

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- Ability to conduct complex digital systems design within an integrated engineering team.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Report 1
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables
- Practical 9
- Practical 10
- Practical 11
- Practical 12
- Project 2 Deliverables
- Report 2

- Exam

## Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

### Learning outcomes

- Ability to apply VHDL programming to the implementation of electronic circuits on FPGAs.
- Ability to conduct complex digital systems design within an integrated engineering team.
- In depth understanding of the characteristics of CMOS technology, the process of CMOS fabrication and the architecture of a microcontroller.

### Assessment tasks

- Report 1
- Practical 5
- Practical 6
- Practical 7
- Practical 8
- Project 1 Deliverables
- Practical 9
- Practical 10
- Practical 11
- Practical 12
- Project 2 Deliverables
- Report 2
- Exam

## Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

## Learning outcome

- Ability to conduct complex digital systems design within an integrated engineering team.

## Assessment tasks

- Practical 9
- Practical 10
- Practical 11
- Practical 12
- Project 2 Deliverables
- Report 2
- Exam