# ELEC643

## Digital Systems Design

S2 Day 2019

*School of Engineering*

## Contents

# General Information

Unit convenor and teaching staff
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Thursday 12pm - 1pm

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Credit points
4

Prerequisites
Admission to MEng

Corequisites

Co-badged status

Unit description
This unit is a sequence of lectures and practical work on digital systems designs, including: behavioural specification and description; architecture and structure design; software/ hardware co-design; technology mapping, verification and test. For greater complexity we choose Field-Programmable Gate Arrays (FPGAs) and a variety of software provided by the manufacturer (Xilinx), including Boolean equations, schematic entry, state machines, and a high-level design language (VHDL), itself supporting a variety of modes. This unit gives students the skills and knowledge needed to design modern digital systems.

## Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

# Learning Outcomes

On successful completion of this unit, you will be able to:

Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
Students will learn how to use Verilog to implement digital circuits on an FPGA.
Students will learn about how to implement digital circuits in complementary metal oxide semiconductor (CMOS) circuits and how this low-level design relates to implementation on FPGAs.

# General Assessment Information

**Grading and passing requirement for unit**

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD).

For further details about grading, please refer below in the policies and procedures section.

**Hurdle Requirements**

The final examination is a hurdle requirement. A grade of 50% or more in the final examination is a condition of passing this unit.

**Late submissions and Re-submissions**

Late submissions will attract a penalty of 10% marks per day. Extenuating circumstances will be considered upon lodgement of a formal notice of disruption of studies.

Re-submissions of work are not allowed.

# Assessment Tasks

| Name | Weighting | Hurdle | Due |
|---|---|---|---|
| Lab 1 | 2% | No | Week 2 |
| Lab 2 | 3% | No | Week 3 |
| Lab 3 | 5% | No | Week 4 |
| Lab 4 | 5% | No | Week 5 |
| Lab 5 | 5% | No | Week 6 |
| Lab 6 | 10% | No | Week 8 |
| Lab 7 | 10% | No | Week 10 |

| Name | Weighting | Hurdle | Due |
|---|---|---|---|
| Lab 8 | 10% | No | Week 12 |
| Final Exam | 50% | Yes | Exam period |

## Lab 1

Due: **Week 2**
Weighting: **2%**

Introduction to FPGA software environment.

On successful completion you will be able to:

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.

## Lab 2

Due: **Week 3**
Weighting: **3%**

A comprehensive guide to FPGA programming.

On successful completion you will be able to:

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Lab 3

Due: **Week 4**
Weighting: **5%**

Counters and 7-segment displays part I.

On successful completion you will be able to:

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.

- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Lab 4

Due: **Week 5**
Weighting: **5%**

Counters and 7-segment displays part II.

On successful completion you will be able to:

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Lab 5

Due: **Week 6**
Weighting: **5%**

State Machines on FPGAs.

On successful completion you will be able to:

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Lab 6

Due: **Week 8**
Weighting: **10%**

Musical Logic.

On successful completion you will be able to:

- Students will gain fundamental knowledge of digital systems with respect to several

different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Lab 7

Due: **Week 10**
Weighting: **10%**

Arithmetic Logic Unit (ALU) design.

On successful completion you will be able to:
- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Lab 8

Due: **Week 12**
Weighting: **10%**

GPS Satellite Searcher.

On successful completion you will be able to:
- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Final Exam

Due: **Exam period**
Weighting: **50%**
**This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)**

Final Exam.

On successful completion you will be able to:

- Students will learn about how to implement digital circuits in complementary metal oxide semiconductor (CMOS) circuits and how this low-level design relates to implementation on FPGAs.

# Delivery and Resources

Refer to iLearn and lecture notes for the unit schedule.

# Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy
- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Grade Appeal Policy
- Complaint Management Procedure for Students and Members of the Public
- Special Consideration Policy *(**Note:** The Special Consideration Policy is effective from 4 December 2017 and replaces the Disruption to Studies Policy.)*

Undergraduate students seeking more policy resources can visit the Student Policy Gateway (https://students.mq.edu.au/support/study/student-policy-gateway). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

If you would like to see all the policies relevant to Learning and Teaching visit Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central).

## Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/study/getting-started/student-conduct

## Results

Results published on platform other than eStudent, (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be

made available in eStudent. For more information visit ask.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

## Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

### Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

## Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

## Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

If you are a Global MBA student contact globalmba.support@mq.edu.au

## IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

# Graduate Capabilities

## Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

### Learning outcomes

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to

a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Assessment tasks

- Lab 2
- Lab 3
- Lab 4
- Lab 5
- Lab 6
- Lab 7
- Lab 8

# Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

## Learning outcomes

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
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## Assessment tasks

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- Lab 2

- Lab 3
- Lab 4
- Lab 5
- Lab 6
- Lab 7
- Lab 8
- Final Exam

## Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

### Learning outcomes

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
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- Lab 2
- Lab 3
- Lab 4
- Lab 5
- Lab 6
- Lab 7
- Lab 8
- Final Exam

# Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

## Learning outcomes

- Students will gain fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.
- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
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## Assessment tasks

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- Lab 4
- Lab 5
- Lab 6
- Lab 7
- Lab 8
- Final Exam

# Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

## Learning outcomes

- Students will gain a conceptual understanding of field programmable gate arrays (FPGAs) and the Verilog hardware description language.
- Students will learn how to use Verilog to implement digital circuits on an FPGA.

## Assessment tasks

- Lab 1
- Lab 2
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- Lab 6
- Lab 7
- Lab 8

# Changes from Previous Offering

The labs and lecture content has completely changed since the last offering. Refer to iLearn and lecture notes for more details.