ELEC242

Digital Circuits and Systems

S2 Day 2019

School of Engineering

Contents

General Information

Unit convenor and teaching staff
Convenor
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Friday 10am-12noon

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Credit points
3

Prerequisites
12cp at 100 level or above including COMP115

Corequisites

Co-badged status

Unit description
This unit aims to provide an introduction to the design and application of digital circuits and systems spanning full-custom CMOS building block circuits at the transistor level through to gate level design and hands-on integrated circuit based prototyping and testing in the laboratory. The unit also aims to provide the students with an understanding of and fluency in the combinational and sequential logic techniques used in the design of large-scale digital systems as well as preparing them for more advanced units on programmable logic design and digital systems.

Important Academic Dates

Information about important academic dates including deadlines for withdrawing from units are available at https://www.mq.edu.au/study/calendar-of-dates

Learning Outcomes

On successful completion of this unit, you will be able to:

Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.
Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.
Build and test prototype logic circuits from integrated circuit components.
Demonstrate understanding of the basic digital full-custom CMOS building block circuits at the transistor level, including: - static, dynamic and switch level CMOS logic circuits, as well as memory elements (such as latches, flip flops and registers) and arithmetic building blocks.

General Assessment Information

Grading and passing requirement for unit

In order to pass this unit a student must obtain a mark of 50 or more for the unit (i.e. obtain a passing grade P/ CR/ D/ HD).

For further details about grading, please refer below in the *policies and procedures* section.

If you receive special consideration for the final exam, a supplementary exam will be scheduled in the supplementary examination period, typically about 3 to 4 weeks after the normal exam period. By making a special consideration application for the final exam you are declaring yourself available for a resit during the supplementary examination period and will not be eligible for a second special consideration approval based on pre-existing commitments. Please ensure you are familiar with the policy prior to submitting an application. Approved applicants will receive an individual notification one week prior to the exam with the exact date and time of their supplementary examination.

Hurdle Requirements

There are two hurdle requirements for passing this unit. The final examination is a hurdle requirement. A grade of 50% or more in the final examination is a condition of passing this unit. If you are given a second opportunity to sit the final examination as a result of failing to meet the minimum mark required, you will be offered that chance during the supplementary examination period and will be notified of the exact day and time after the publication of final results for the unit. The second attempt at a hurdle assessment is graded as pass fail. The maximum grade for a second attempt is the hurdle threshold grade.

Participation in practical sessions is a hurdle requirement and students are required to attend at least 10/12 practical sessions to pass this unit

Late submissions and Resubmissions

Late submissions will attract a penalty of 20/100 marks per day. Extenuating circumstances will

be considered upon lodgement of a formal notice of request for *Special Consideration*.

Resubmissions of work are not allowed.

Assessment Tasks

Name	Weighting	Hurdle	Due
Student Engagement	10%	Yes	Continuous
Simple Design	10%	No	Week 5
Design Assignment	20%	No	Week 9
Unit Exam	60%	Yes	TBA

Student Engagement

Due: **Continuous**
Weighting: **10%**
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

Students are expected to actively participate in the learning activities with a developing level of independence as well as group work. Further, before each practical, the students will be given pre-practical preparation work which they must complete before attending the practicals. Grading of this aspect will take into consideration the pre-practical preparation work completion and the level of participation.

On successful completion you will be able to:

- Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.
- Build and test prototype logic circuits from integrated circuit components.

Simple Design

Due: **Week 5**
Weighting: **10%**

This is the first design assignment. You will take the knowledge about digital circuits presented so far and design a circuit to perform a given task.

Submission will be through ilearn.

On successful completion you will be able to:

- Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.

- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.

Design Assignment

Due: **Week 9**
Weighting: **20%**

This assignment is a design assignment. You must present the design for a state machine to solve the project outline given. A rubric will be issued to indicate what is being looked for in the assignment.

Submission will be through ilearn.

On successful completion you will be able to:

- Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.
- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.

Unit Exam

Due: **TBA**
Weighting: **60%**
This is a hurdle assessment task (see assessment policy for more information on hurdle assessment tasks)

There is a formal examination of the material covered in the pre-work, laboratory work, and lecture material presented during the unit. This is a hurdle assessment. You must pass the exam to be eligible to pass the unit. The exam is scheduled to last three hours.

On successful completion you will be able to:

- Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.
- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.

- Build and test prototype logic circuits from integrated circuit components.
- Demonstrate understanding of the basic digital full-custom CMOS building block circuits at the transistor level, including: - static, dynamic and switch level CMOS logic circuits, as well as memory elements (such as latches, flip flops and registers) and arithmetic building blocks.

Delivery and Resources

Lectures	There is one lecture per week. Attendance is highly recommended at all lectures. Announcements and feedback will be made in lectures.
Laboratory Note Book	Each student is required to have a bound laboratory notebook. This book must have all required pre-work recorded. It must also contain all your development work during the project, and must be made available on request.
Recommended Text	Thomas L. Floyd, Digital Fundamentals (10^{th} Edition or later) This book is recommended, not required.

Unit Schedule

Practicals will commence in Week 2.

Policies and Procedures

Macquarie University policies and procedures are accessible from Policy Central (https://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central). Students should be aware of the following policies in particular with regard to Learning and Teaching:

- Academic Appeals Policy
- Academic Integrity Policy
- Academic Progression Policy
- Assessment Policy
- Fitness to Practice Procedure
- Grade Appeal Policy
- Complaint Management Procedure for Students and Members of the Public
- Special Consideration Policy *(**Note:** The Special Consideration Policy is effective from 4 December 2017 and replaces the Disruption to Studies Policy.)*

Undergraduate students seeking more policy resources can visit the Student Policy Gateway (https://students.mq.edu.au/support/study/student-policy-gateway). It is your one-stop-shop for the key policies you need to know about throughout your undergraduate student journey.

If you would like to see all the policies relevant to Learning and Teaching visit Policy Central (http

s://staff.mq.edu.au/work/strategy-planning-and-governance/university-policies-and-procedures/policy-central).

Student Code of Conduct

Macquarie University students have a responsibility to be familiar with the Student Code of Conduct: https://students.mq.edu.au/study/getting-started/student-conduct

Results

Results published on platform other than eStudent, (eg. iLearn, Coursera etc.) or released directly by your Unit Convenor, are not confirmed as they are subject to final approval by the University. Once approved, final results will be sent to your student email address and will be made available in eStudent. For more information visit ask.mq.edu.au or if you are a Global MBA student contact globalmba.support@mq.edu.au

Student Support

Macquarie University provides a range of support services for students. For details, visit http://students.mq.edu.au/support/

Learning Skills

Learning Skills (mq.edu.au/learningskills) provides academic writing resources and study strategies to improve your marks and take control of your study.

- Workshops
- StudyWise
- Academic Integrity Module for Students
- Ask a Learning Adviser

Student Services and Support

Students with a disability are encouraged to contact the Disability Service who can provide appropriate help with any issues that arise during their studies.

Student Enquiries

For all student enquiries, visit Student Connect at ask.mq.edu.au

If you are a Global MBA student contact globalmba.support@mq.edu.au

IT Help

For help with University computer systems and technology, visit http://www.mq.edu.au/about_us/offices_and_units/information_technology/help/.

When using the University's IT, you must adhere to the Acceptable Use of IT Resources Policy. The policy applies to all who connect to the MQ network including students.

Graduate Capabilities

Creative and Innovative

Our graduates will also be capable of creative thinking and of creating knowledge. They will be imaginative and open to experience and capable of innovation at work and in the community. We want them to be engaged in applying their critical, creative thinking.

This graduate capability is supported by:

Learning outcomes

- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.
- Build and test prototype logic circuits from integrated circuit components.

Assessment tasks

- Student Engagement
- Design Assignment
- Unit Exam

Capable of Professional and Personal Judgement and Initiative

We want our graduates to have emotional intelligence and sound interpersonal skills and to demonstrate discernment and common sense in their professional and personal judgement. They will exercise initiative as needed. They will be capable of risk assessment, and be able to handle ambiguity and complexity, enabling them to be adaptable in diverse and changing environments.

This graduate capability is supported by:

Learning outcomes

- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.
- Build and test prototype logic circuits from integrated circuit components.

Assessment tasks

- Student Engagement
- Design Assignment
- Unit Exam

Commitment to Continuous Learning

Our graduates will have enquiring minds and a literate curiosity which will lead them to pursue knowledge for its own sake. They will continue to pursue learning in their careers and as they participate in the world. They will be capable of reflecting on their experiences and relationships

with others and the environment, learning from them, and growing - personally, professionally and socially.

This graduate capability is supported by:

Learning outcomes

- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.
- Build and test prototype logic circuits from integrated circuit components.

Assessment tasks

- Student Engagement
- Design Assignment
- Unit Exam

Discipline Specific Knowledge and Skills

Our graduates will take with them the intellectual development, depth and breadth of knowledge, scholarly understanding, and specific subject content in their chosen fields to make them competent and confident in their subject or profession. They will be able to demonstrate, where relevant, professional technical competence and meet professional standards. They will be able to articulate the structure of knowledge of their discipline, be able to adapt discipline-specific knowledge to novel situations, and be able to contribute from their discipline to inter-disciplinary solutions to problems.

This graduate capability is supported by:

Learning outcomes

- Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.
- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.
- Build and test prototype logic circuits from integrated circuit components.
- Demonstrate understanding of the basic digital full-custom CMOS building block circuits at the transistor level, including: - static, dynamic and switch level CMOS logic circuits, as well as memory elements (such as latches, flip flops and registers) and arithmetic building blocks.

Assessment tasks

- Student Engagement
- Simple Design
- Design Assignment
- Unit Exam

Critical, Analytical and Integrative Thinking

We want our graduates to be capable of reasoning, questioning and analysing, and to integrate and synthesise learning and knowledge from a range of sources and environments; to be able to critique constraints, assumptions and limitations; to be able to think independently and systemically in relation to scholarly activity, in the workplace, and in the world. We want them to have a level of scientific and information technology literacy.

This graduate capability is supported by:

Learning outcomes

- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.
- Build and test prototype logic circuits from integrated circuit components.
- Demonstrate understanding of the basic digital full-custom CMOS building block circuits at the transistor level, including: - static, dynamic and switch level CMOS logic circuits, as well as memory elements (such as latches, flip flops and registers) and arithmetic building blocks.

Assessment tasks

- Student Engagement
- Simple Design
- Design Assignment
- Unit Exam

Problem Solving and Research Capability

Our graduates should be capable of researching; of analysing, and interpreting and assessing data and information in various forms; of drawing connections across fields of knowledge; and they should be able to relate their knowledge to complex situations at work or in the world, in order to diagnose and solve problems. We want them to have the confidence to take the initiative in doing so, within an awareness of their own limitations.

This graduate capability is supported by:

Learning outcomes

- Specify and minimise combinational logic functions using Boolean algebra as well as Karnaugh-map techniques.
- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
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Assessment tasks

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Effective Communication

We want to develop in our students the ability to communicate and convey their views in forms effective with different audiences. We want our graduates to take with them the capability to read, listen, question, gather and evaluate information resources in a variety of formats, assess, write clearly, speak effectively, and to use visual communication and communication technologies as appropriate.

This graduate capability is supported by:

Learning outcomes

- Specify synchronous sequential behaviour in terms of a state diagram and design, from a state diagram, synchronous sequential circuits, including arbitrary-sequence counters and simple finite-state-machines, using D-type flip-flops.
- Design fast and efficient combinational logic circuits at gate level using mixed logic techniques.

Assessment tasks

- Simple Design
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Engaged and Ethical Local and Global citizens

As local citizens our graduates will be aware of indigenous perspectives and of the nation's historical context. They will be engaged with the challenges of contemporary society and with knowledge and ideas. We want our graduates to have respect for diversity, to be open-minded, sensitive to others and inclusive, and to be open to other cultures and perspectives: they should have a level of cultural literacy. Our graduates should be aware of disadvantage and social justice, and be willing to participate to help create a wiser and better society.

This graduate capability is supported by:

Learning outcome

- Demonstrate understanding of the basic digital full-custom CMOS building block circuits at the transistor level, including: - static, dynamic and switch level CMOS logic circuits, as well as memory elements (such as latches, flip flops and registers) and arithmetic building blocks.

Assessment task

- Unit Exam

Socially and Environmentally Active and Responsible

We want our graduates to be aware of and have respect for self and others; to be able to work with others as a leader and a team player; to have a sense of connectedness with others and country; and to have a sense of mutual obligation. Our graduates should be informed and active participants in moving society towards sustainability.

This graduate capability is supported by:

Learning outcome

- Demonstrate understanding of the basic digital full-custom CMOS building block circuits at the transistor level, including: - static, dynamic and switch level CMOS logic circuits, as well as memory elements (such as latches, flip flops and registers) and arithmetic building blocks.

Assessment task

- Unit Exam

Changes from Previous Offering

The major project will change, and a new trainer board has been developed, allowing more hands on work rather than pure theory.

Changes in Response to Student Feedback

Additional hands on work is being provided through the new trainer boards.